ESCOLA POLITÉCNICA DA UNIVERSIDADE DE SÃO PAULO

DEPARTAMENTO DE ENGENHARIA MECÂNICA

TRABALHO DE FORMATURA

"RETRO-FITTING E ANÁLISE DE UMA MÁQUINA DE ENSAIO DE TRAÇÃO"

PAULO FIGUEIREDO CHEIDA MOTA

ORIENTADOR : PROFESSOR DR. VALTER F. A. ALVES

1996

Aos meus pais.

AGRADECIMENTOS

A todos que contribuíram com a realização deste trabalho, especialmente:

Ao professor Valter, pela orientação;

Aos funcionários da Iochpe-Maxion S.A. - Divisão de Motores;

A Luís Eduardo Vicente Catta-Preta, supervisor da Garantia da Qualidade pela oportunidade profissional única;

Aos Técnicos do Laboratório de Metrologia e Metalurgia da Iochpe-Maxion;

Aos funcionários da Instrumentação da Iochpe-Maxion, que me forneceram os recursos para a minha pesquisa;

Aos professores e funcionários da Escola Politécnica;

A minha família, pela compreensão e apoio.

SUMÁRIO

Este trabalho tem como objetivo projetar um sistema de aquisição de dados confiável e de baixo custo para uso em uma máquina de ensaio de tração.

Após a avaliação inicial, foi constatado que, com componentes comuns, facilmente encontrados no mercado, é possível construir um sistema de aquisição de sinais simples, adequado às necessidades do projeto.

Grande parte das tarefas da aquisição de dados - controle do equipamento, tratamento do sinal - pode ser realizado por software, tornando desnecessário a inclusão de circuitos adicionais de controle na placa, reduzindo o custo final do equipamento.

RESUMO

No capítulo 1 são expostos os motivos da realização do trabalho, as necessidades práticas e os recursos disponíveis à época do início do projeto.

No capítulo 2, o problema é inicialmente analisado, com levantamento de especificações e modelagem. Algumas soluções são propostas e analisadas criticamente. A solução que será estudada de forma mais aprofundada é escolhida.

No capítulo 3 é executado o projeto da solução escolhida no capítulo anterior. É projetado e construído um protótipo de uma placa de aquisição de sinais analógicos, para a automação das medições.

No capítulo 4 é feita a conclusão do trabalho, assim como considerações surgidas após a realização deste.

ÍNDICE

CAPÍTULO 1 -INTRODUÇÃO

1.1 - APRESENTAÇÃO DO PROBLEMA

O laboratório metalúrgico da Divisão de Motores da Iochpe-Maxion S.A. possui uma máquina de ensaio universal modelo RH-30 TU [Figura 1] fabricada pela SHIMADZU.

A máquina de ensaio é do tipo "mole", de acionamento hidráulico. O movimento da máquina é acionado por uma bomba radial de 7 pistões [Figura 2]. O fluido hidráulico movimenta o êmbolo que faz subir a mesa. A máquina é capaz de fazer dois tipos de ensaio: o cabeçote superior da máquina faz os ensaios de tração, enquanto que o cabeçote inferior realiza os de compressão [Figura 3].

Capacidade da máquina : 30 toneladas.

Curso máximo do ensaio : 200 mm.

Dados: [SHIMADZU]

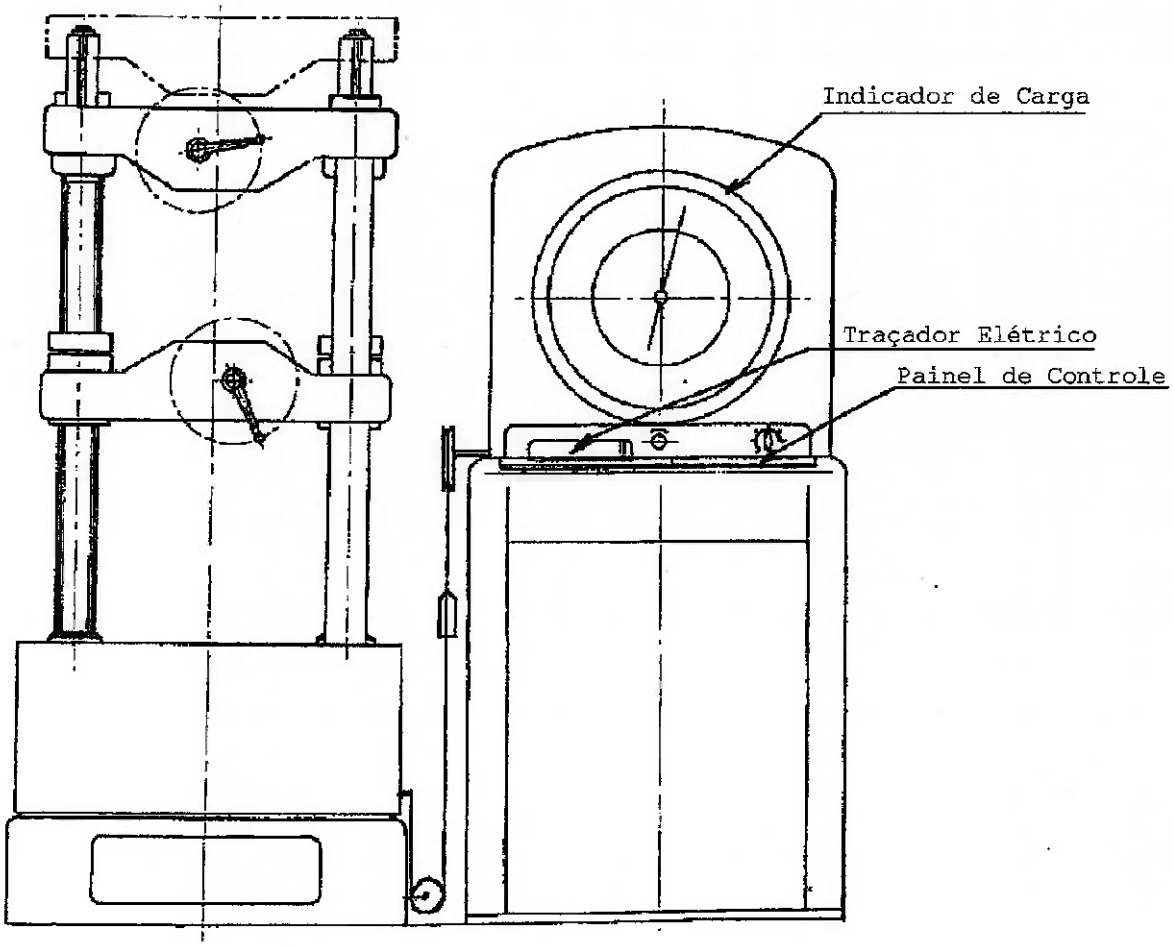


Figura 1 - Máquina - [SHIMADZU]

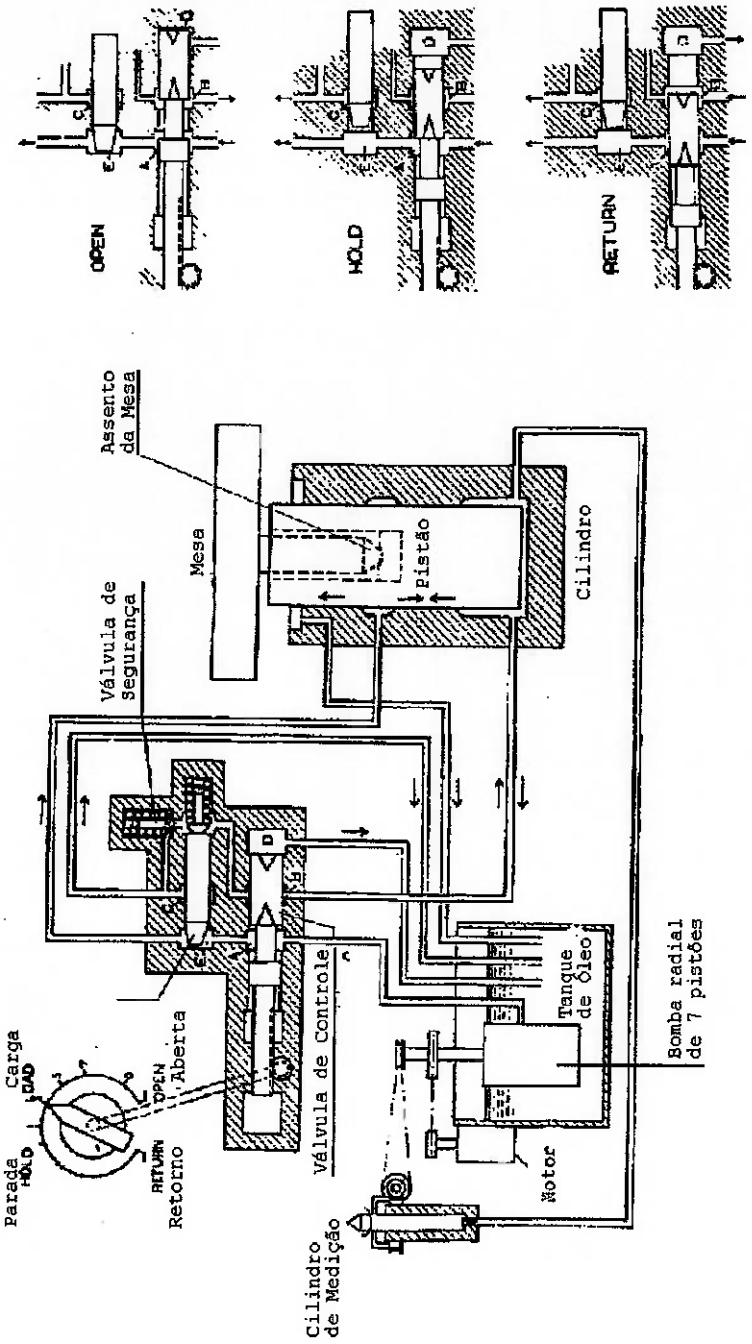


Figura 2 - Bomba e mecanismo hidráulico [SHIMADZU]

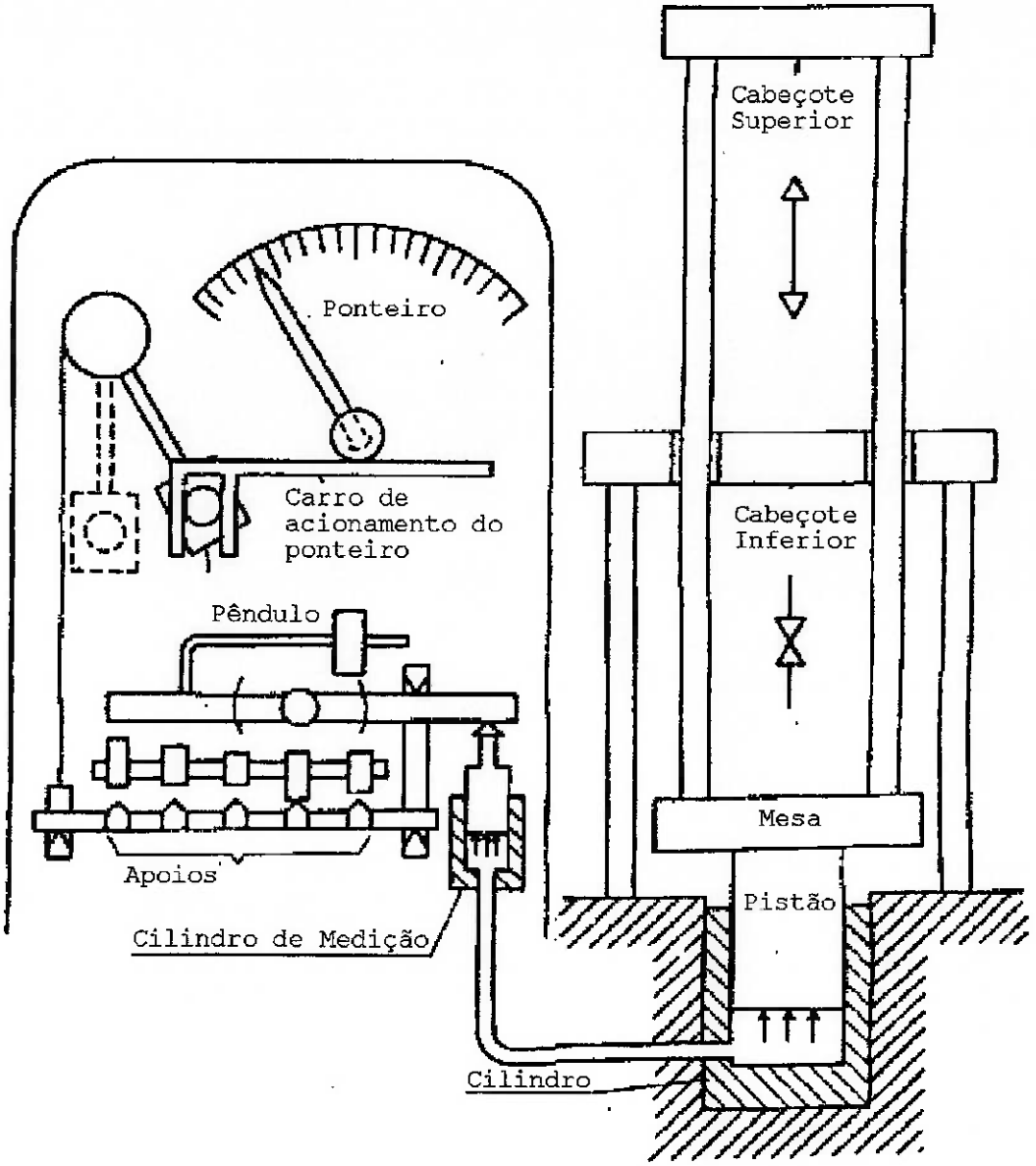


Figura 3 - Mecanismo hidráulico [SHIMADZU]

A máquina possui um traçador eletro-mecânico para obter a curva tensão-deslocamento em um gráfico. Este traçador é composto de um cilindro movido por meio de um cabo ligado à mesa e uma pena conectada eletricamente ao sensor de pressão hidráulica da máquina. Este sistema não permite uma resolução satisfatória das deformações, já que uma amplificação mecânica resultaria em perda de precisão.

Nas atividades do laboratório metalúrgico da empresa, os objetivos principais dos ensaios são a medição da resistência e dos limites de escoamento e de ruptura, para fins de inspeção de amostras destinadas à produção.

Para a medição do limite de ruptura, a máquina apresenta desempenho satisfatória, pois para isso é suficiente apenas a leitura do ponteiro de arraste do medidor de carga, que indica a tensão máxima suportada pela amostra.

Na medição do elongamento de materiais resistentes, o traçador não permite uma boa verificação da inclinação da curva tensão-deformação, pelo deslocamento ser muito pequeno, e a amplificação mecânica deste deslocamento não ser satisfatória. O mesmo problema ocorre para materiais que tem o limite de escoamento pouco definido, quando é

necessário obter a tensão pela curva do elongamento de 0,2%.

Para resolver estes problemas, atualmente recorre-se ao uso de um strain-gage colado ao corpo de prova [Figura 4] ou de um clip-gage, sendo a medição sendo feita passo a passo, variando-se a carga e anotando os resultados manualmente. Este método é muito demorado e passível de erro. São necessários dois operadores para realizar a medição. Além disso, poucos pontos são obtidos.

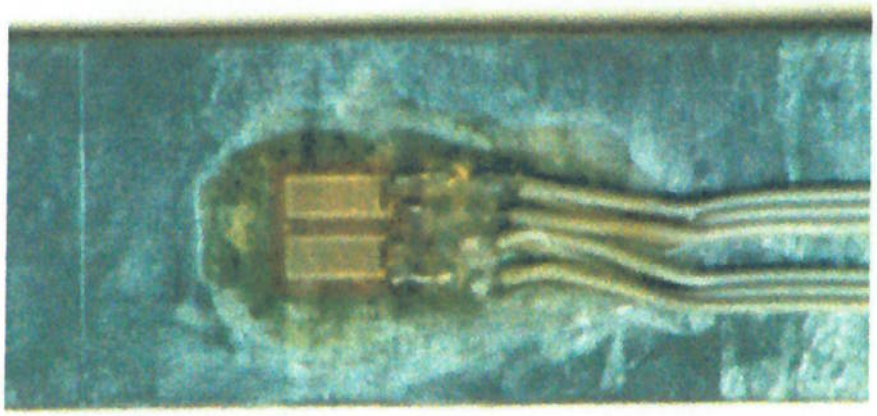


Figura 4 - Strain Gage

1.2 - ESTABELECIMENTO DA NECESSIDADE

É preciso, com o aproveitamento da máquina existente, a adaptação de um sistema de controle e medição em tempo real para execução dos ensaios. Em um único passo, devem ser obtidos a resistência, o limite de elongamento e o limite de ruptura.

O sistema deve dar suporte a ensaios repetitivos. Os dados referentes aos ensaios devem ser armazenados para análise estatística de lote. A interferência do operador nos ensaios deve ser a mínima possível.

As alterações estruturais na máquina devem ser mínimas, para evitar o comprometimento da precisão da máquina. A máquina passa por aferições anuais realizadas por empresa de metrologia externa.

O custo da instalação deve ser o menor possível, com aproveitamento de materiais e recursos disponíveis na empresa.

CAPÍTULO 2 - A ESCOLHA DO PROJETO

Os procedimentos para o projeto podem ser encontrados em [MADUREIRA, 1993].

2.1 - CARACTERÍSTICAS DO PROJETO

Características funcionais

a) Desempenho : medição contínua da tensão e do deslocamento, controle automático da pressão hidráulica, ensaios repetitivos automáticos. Precisão de 0.005 mm na medição dos deslocamentos.

b) Segurança : parada de emergência automática da máquina em caso de pane no controlador. Limitador de curso da mesa. Impedimento da quebra do strain-gage.

Características operacionais

a) Durabilidade : vida útil dos componentes de pelo menos 4 anos.

b) Confiabilidade : manutenção da precisão entre aferições anuais.

2.2 - FORMULAÇÃO DO SISTEMA

Entradas desejáveis:

- dimensões do corpo de prova
- geometria do corpo de prova
- material do corpo de prova
- tamanho do lote a ser ensaiado

Saídas desejáveis (objetivos):

- gráfico tensão-deformação
- obtenção dos limites de escoamento e resistência
- análise estatística do lote
- comunicação de dados com outro computador

Entradas indesejáveis:

- erros na informação sobre o corpo de provas

- ensaio realizado sem o corpo de provas

- queda na alimentação do controlador

Saídas indesejáveis:

- quebra do strain-gage

- excesso de pressão hidráulica no sistema

2.3 - SÍNTESE DE SOLUÇÕES

Funções		Alternativas	
	A	B	C
1. Controle do sistema	Microcomputador	Microcomputador	Placa Microprocessada com comunicação para Microcomputador
2. Medição do deslocamento	Strain-Gage + LVDT	Strain-Gage + Polia e Potenciômetro	Strain-Gage + Régua Resistiva
3. Medição das tensões	Sinal do registrador elétrico	Potenciômetro conectado ao eixo do ponteiro indicador da carga	Transdutor de pressão
4. Controle da carga	Motor DC atuando na válvula já existente	Servo-Válvula	Válvula proporcional + controlador PID
5. Aquisição dos dados	Condicionador de Sinais + Amplificador + Placa A/D	Amplificador + Placa A/D	Amplificador + Placa A/D
6. Saída do sinal de controle da carga	Relés	Placa D/A + Amplificador	Placa D/A + Amplificador

Solução A:

O laboratório tem disponível um microcomputador compatível com IBM PC-XT, usado. É preferível implementar o sistema em uma linguagem de fácil depuração como Turbo Pascal, a programar uma placa de controle em código de máquina. A comunicação dos sensores e atuadores (conversor D/A, amplificadores, relés) com o computador deve ser implementada em placas conectadas aos slots.

Foi considerado o aproveitamento da medida da pressão hidráulica já existente, utilizada pelo registrador elétrico. O sinal deve ser condicionado por um amplificador para ficar compatível com o conversor A/D.

A medida das deformações, para pequenos deslocamentos será feito com um clip-gage fixado ao corpo de prova. A saída elétrica passa por um amplificador e é amostrada pelo conversor A/D. Para grandes deslocamentos, a posição é medida por um LVDT e o sinal é alimentado no A/D por um condicionador.

O controle da carga é feito por um motor elétrico com redutor, acionando a válvula de controle hidráulica. O computador aciona motor através de uma placa de relés. Sensores de fim de curso impedem

que se exceda o ângulo máximo de acionamento. A posição da válvula é medida por um potenciômetro linear, conectado ao conversor A/D. O esquema da solução A está representado na figura 5.

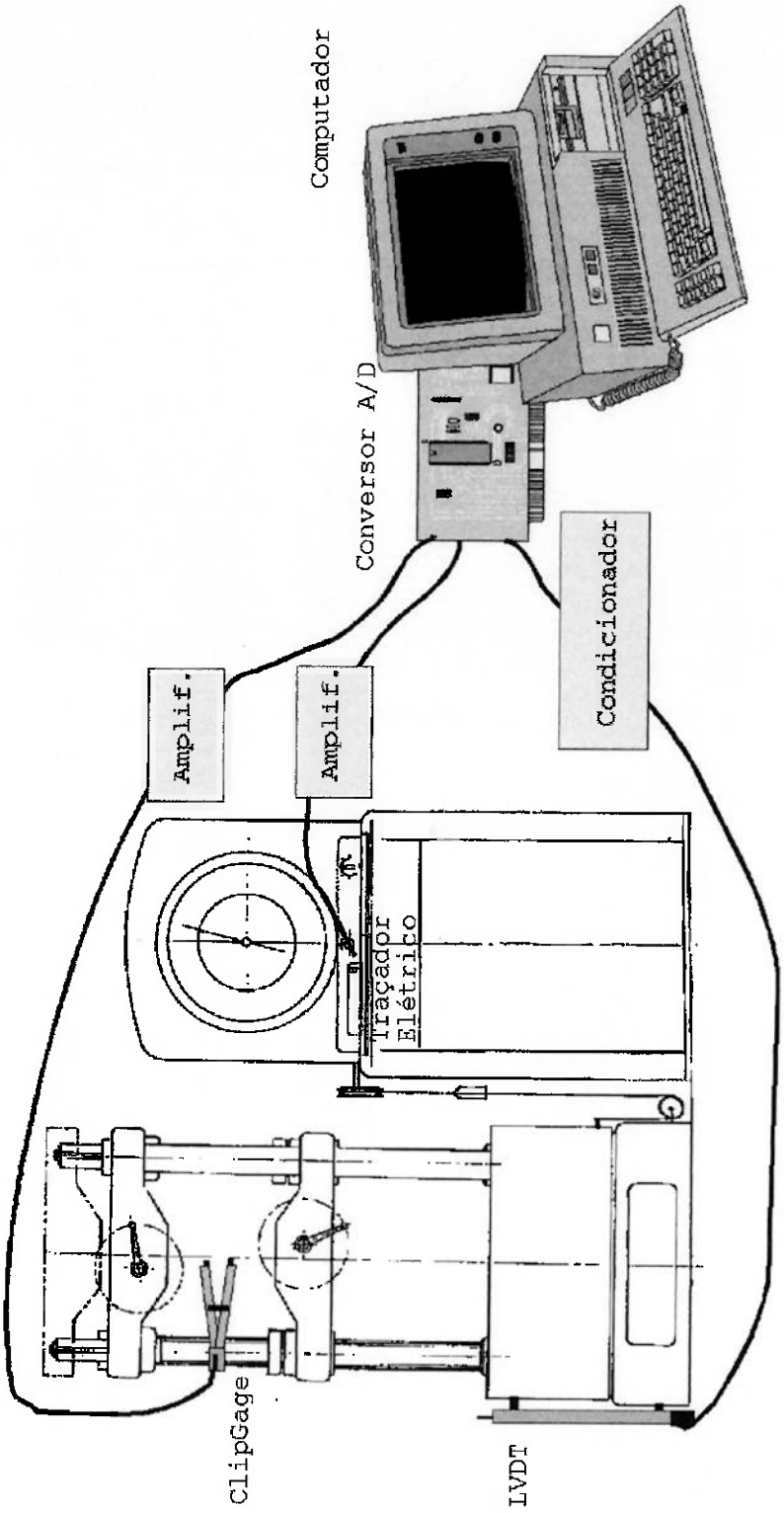


Figura 5 - Solução A

Solução B:

Assim como a solução A, também tem o controle do sistema feito pelo computador.

Para medir a carga, é utilizado um potenciômetro conectado ao eixo do ponteiro da máquina. Como é possível a mudança da escala, devem ser obtida por meio de um switch rotativo a escala de carga sendo indicada pelo ponteiro.

A medida das deformações, para pequenos deslocamentos será feito com um clip-gage fixado ao corpo de prova. A saída elétrica passa por um amplificador e é amostrada pelo conversor A/D. Para grandes deslocamentos, a posição é medida por um potenciômetro ligado ao eixo da polia que acionava o registrador elétrico.

O controle de carga é feito utilizando-se uma servo-válvula. O sinal de alimentação da válvula é gerado digitalmente pelo computador, convertido por um D/A e depois amplificado.

O esquema da solução B pode ser visto na Figura 6.

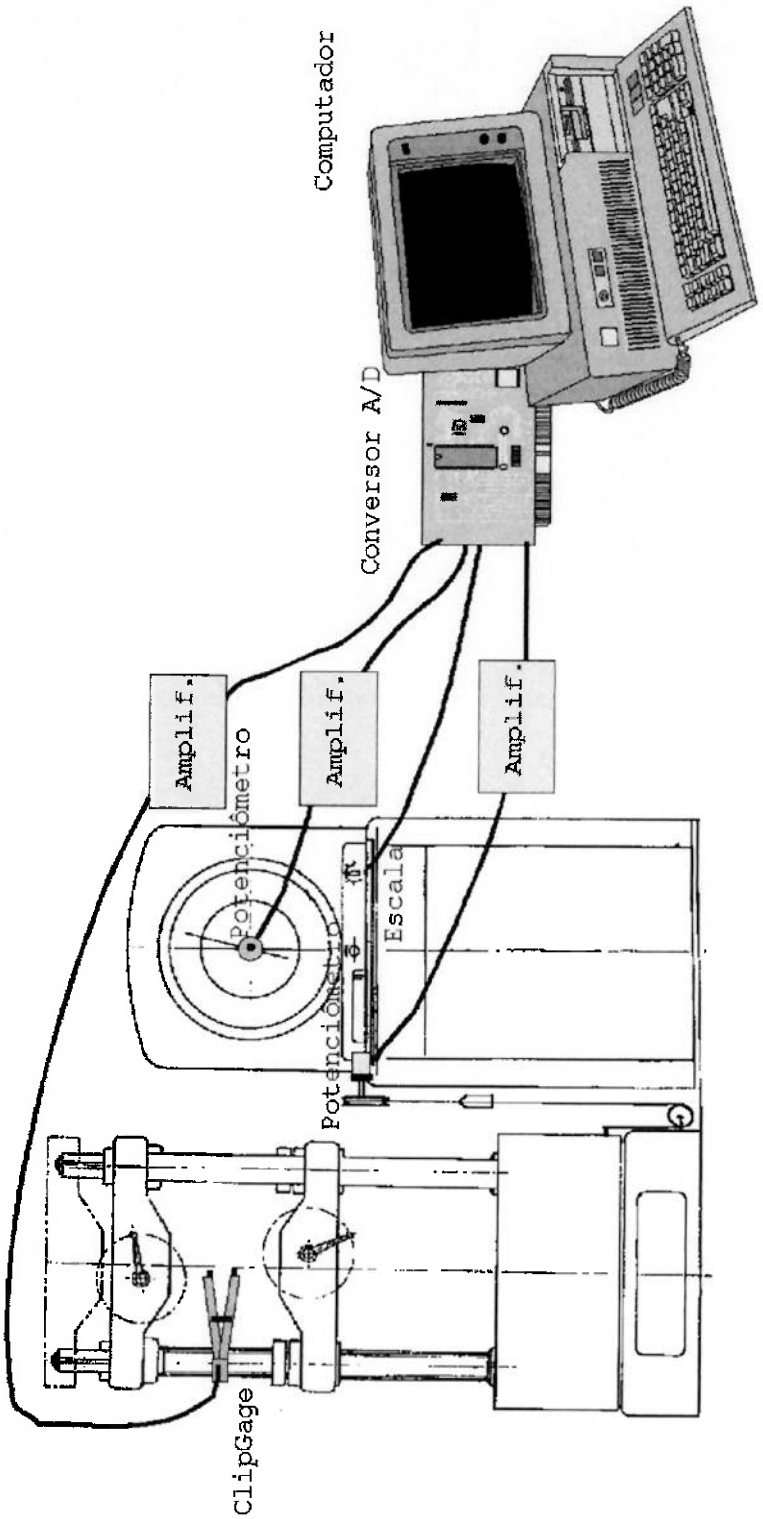


Figura 6 - Solução B

Solução C:

Para o controle do sistema deve ser projetado um controlador microprocessado com interface para microcomputador. O controlador deve possuir em seu programa ciclos de diagnóstico e calibração. A principal vantagem do controlador é dos testes serem efetuados independentemente do tratamento dos dados, por não haver ocupação do computador com o controle.

A carga deve ser medida por um transdutor de pressão conectado ao sistema hidráulico. O próprio sinal do transdutor serve de alimentação para o controle da válvula proporcional, que controla a carga.

A medida das deformações, para pequenos deslocamentos será feito com um clip-gage fixado ao corpo de prova. A saída elétrica passa por um amplificador e é amostrada pelo conversor A/D. Para grandes deslocamentos, a posição é medida por uma régua resistiva. A Figura 7 representa a solução C.

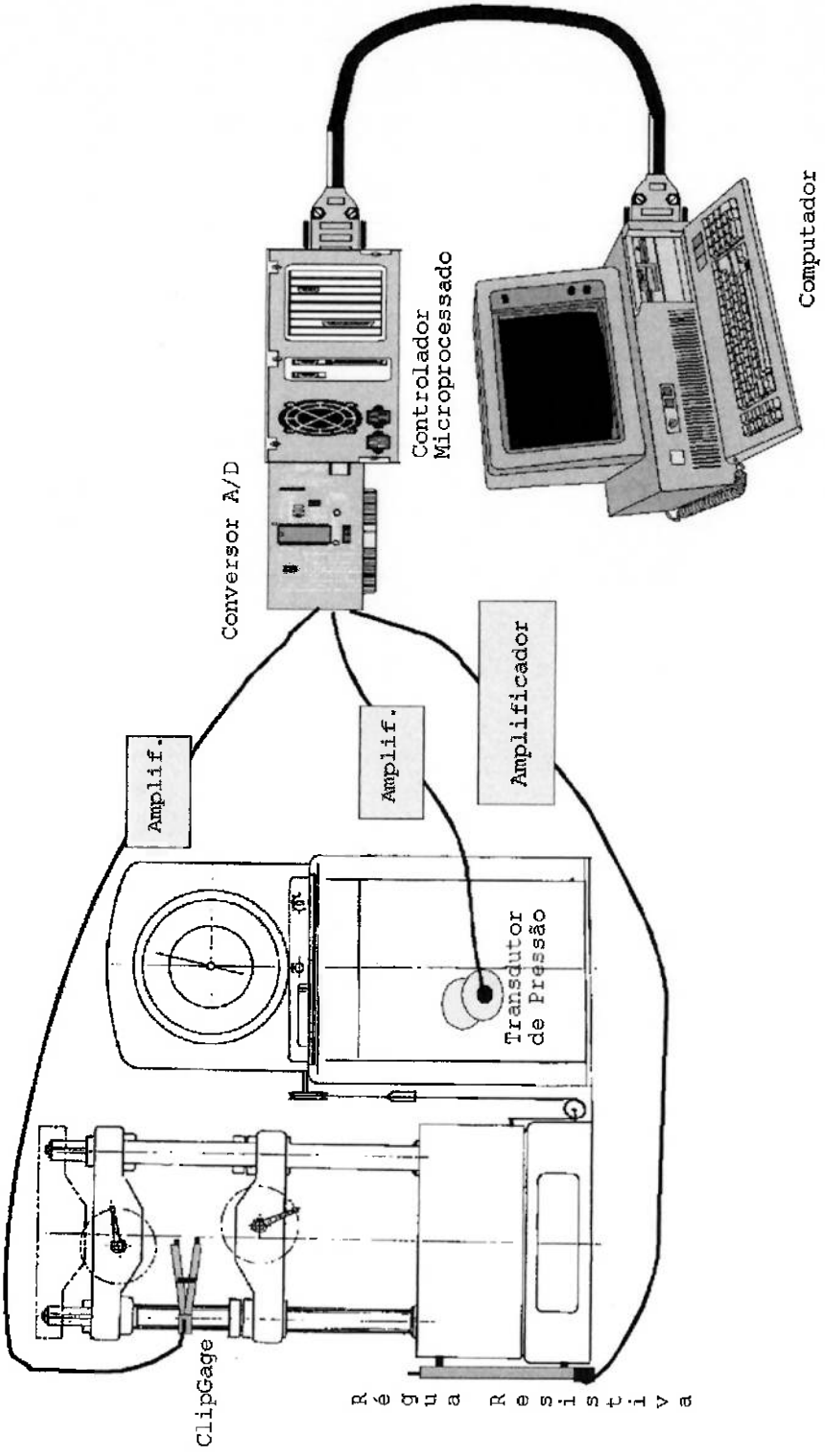


Figura 7 - Solução C

2.4 - ESCOLHA DA MELHOR SOLUÇÃO

A solução C foi descartada em razão da complexidade e custo.

A placa microprocessada requer um gasto muito grande com o projeto de hardware e software. A conexão do transdutor de pressão e da válvula de controle exige grandes mudanças na tubulação da máquina e pode alterar seu comportamento e capacidade. A régua resistiva pode não resistir ao choque que a máquina sofre na ruptura do corpo de prova.

As soluções A e B são aceitáveis, desde que a precisão obtida na medição do deslocamento seja de 0,005 mm.

Na solução A, pode ser empregado um LVDT com curso linear de 20,000 mm.

Na solução B, caso se utilize a polia original, de 90 mm de diâmetro, o comprimento para uma volta é de 282,74 mm. Para obter 0,005 mm de resolução, a precisão do potenciômetro deveria ser de 0,00637 graus, impossível de ser alcançada. (1 grau = 0,799 mm). Se é utilizada uma polia menor, deve ser considerado o efeito do diâmetro do fio, não desprezível.

O objetivo é ter uma definição de 20 pontos para 0,2% de elongamento de um corpo de prova de 50 mm de comprimento útil.

50 mm x 0,2% = 0,1 mm. 0,1 mm = 20 pontos => 1 ponto = 0,005 mm.

A placa A/D disponível é de 12 bits, com resolução de 4096 pontos. Portanto, para uma resolução de 0,005 mm, o máximo comprimento mensurável é de 20,48 mm.

No projeto básico deverá também ser considerado o uso de um conversor A/D de 16 bits. Para não haver erros na obtenção das curvas de força e deslocamento, os sinais devem ser amostrados simultaneamente por meio de "sample-hold". Precisão de Medição : 0,005 mm, para um comprimento de amostra máximo de 200 mm; 0,5 Kgf para carga, de um máximo de 30 Tf.

Conclusão:

A necessidade real do laboratório é a obtenção dos resultados dos ensaios em forma gráfica com uma precisão razoável. Os funcionários do laboratório precisam de relatórios que indiquem a condição do lote.

O laboratório faz análise de componentes comprados externamente e produzidos na fábrica. A maior

dificuldade nos ensaios é a obtenção do valor dos limites convencionais de escoamento (0,2% , 0,5%), que são indicados nas especificações dos materiais das peças.

Não há necessidade de análises estatísticas complexas nas amostras, uma vez que o laboratório apenas se preocupa em constatar a conformidade ou não de um determinado lote.

Para a escolha definitiva do projeto, as características da solução escolhida previamente, Solução "A", serão reavaliadas, adequando melhor o projeto às necessidades e possibilidades de execução. A solução mais adequada é a A, devendo ser mais detalhada no projeto básico.

CAPÍTULO 3 - EXECUÇÃO DO PROJETO.

3.1 - ESPECIFICAÇÃO DO PROJETO.

Automação das Medições:

É preciso que o registro das medições seja automático, que o operador não necessite anotar os valores. O processo do ensaio não necessita ser totalmente automático, pois sempre é necessária a presença do operador, por questões de segurança.

Capacidade de Calcular:

Quando solicitado, deve fornecer os valores da tensão máxima, e calcular o limite de escoamento automaticamente.

Facilidade de Operação:

A máquina com o novo sistema não deve ser mais complicado ou demandar mais tempo para operar do que no estado original.

Segurança:

Se não há condições de prevenir, ao menos a máquina não deve ter disposição ou possibilidade de provocar acidentes.

Apresentação:

A aparência deve apresentar e transmitir confiança.

Espaço Ocupado:

O espaço do laboratório é reduzido e caro para a empresa, por ser considerado "área não produtiva".

Custo:

O volume de recursos despendidos com o projeto, deve ser o menor possível.

3.2 - ANÁLISE DETALHADA DA SOLUÇÃO.

Controle do sistema por Microcomputador. O microcomputador já é possuído pelo laboratório e encontra-se atualmente sem utilização. (Custo baixo). Os recursos já presentes no computador podem ser utilizados (Armazenamento de resultados, possibilidade de comunicação com outras máquinas, conexão com impressora), reduzindo ainda mais o custo e o espaço ocupado. A complexidade de se projetar e fazer placas de aquisição de sinais e controle é muito menor do que a de se projetar uma placa microprocessada (praticamente o projeto de um computador).

Medição do deslocamento por Strain-Gage + LVDT. Um clip-gage, com seu próprio condicionador de sinais e display já está disponível. A saída elétrica do condicionador de sinais é da ordem de 1 mV. Este sinal deve ser amplificado para a aquisição pela placa. Este sistema é o mais adequado para pequenos deslocamentos, como o ensaio para se obter os limites convencionais de escoamento. Pelas suas características de fixação, pode se garantir a medida comprimento do corpo de prova que está se deformando devido à tensão.

O LVDT, para esta máquina, é inadequado para medir grandes deslocamentos. Um transdutor linear de posição (Régua resistiva de pista plástica) [Figura 8] possibilita maiores deslocamentos, sem a necessidade de circuitos de apoio complexos.

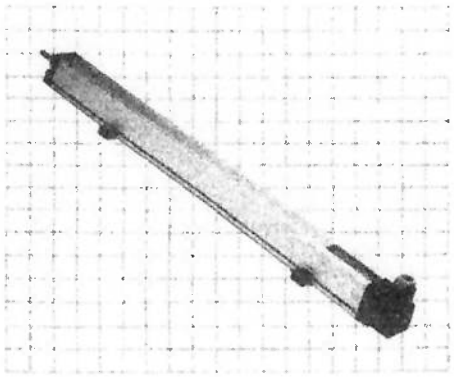


Figura 8 - Transdutor Linear de Posição modelo LT [GEFRAN BRASIL]

Controle da carga : a automação total das medidas foge ao propósito deste estudo. O laboratório não necessita de uma máquina que funcione sozinha, pois o volume de amostras analisadas é pequeno. Apenas é preciso que os dados sejam coletados assim que a máquina é operada, sem a intervenção do operador.

Medição das tensões: o sinal do traçador elétrico não deve ser utilizado, uma vez que não é considerado confiável, tendo em vista a idade da máquina. Para medir as tensões, deve ser utilizado um transdutor de pressão [Figura 9][GEFRAN, modelo TP]. O valor da pressão indicada deve ser transformada em força.

Figura 9 - Transdutor de Pressão série TP
[GEFRAN BRASIL]

Aquisição dos dados: não sendo utilizado o LVDT, não há a necessidade de um condicionador de sinais especializado para ele. Os sinais que estão em milivolts ou em pequenos valores de corrente devem ser amplificados. Para a transferência de dados para o microcomputador será usada uma placa conversora

Analógica/Digital, que converte as grandezas em Volts para valores em bits (valores discretos).

Saída do sinal de controle da carga: o controle da carga será manual. O operador deverá parar a máquina para retirar o clip-gage do corpo de prova antes de prosseguir com o ensaio.

3.3 - PROJETO DO PROTÓTIPO

O protótipo para aquisição de dados é uma placa conversora Analógica/Digital, com possibilidade de ler dados de até 8 canais.

O ponto de partida para o projeto da placa é o Circuito Integrado ADC574A [BURR-BROWN], conversor A/D com 12 bits de resolução. Este circuito, fabricado pela Burr-Brown tem um tempo de conversão mínimo de 25 ms, adequado para a aplicação. Pode ser alimentado com +-12V, disponível da fonte do computador. Comunica-se com o barramento do computador com 8 ou 12 bits por vez.

Para estabilizar o sinal a ser convertido, é utilizado um Circuito Integrado SHC298A [BURR-BROWN], Sample/Hold analógico, que armazena o sinal amostrado em um capacitor pelo tempo necessário para o circuito A/D fazer a conversão. O circuito SCH298A permite que o sinal amostrado tenha precisão de 12 bits, sendo compatível com o conversor.

Para selecionar a fonte do sinal amostrado, o circuito MC14051 [MOTOROLA], multiplexador analógico, possibilita o chaveamento em estado sólido, sem introduzir ruídos no sinal.

O circuito 74LS373 [TEXAS INSTRUMENTS], mantém os sinais de controle da placa mesmo quando ela não está sendo acessada pelo programa.

O circuito 74LS244 [TEXAS INSTRUMENTS] impede que o barramento do conversor A/D entre em curto com o computador, isolando e só permitindo a passagem de sinal quando o programa solicita a leitura do conversor.

O circuito decodificador de endereços, controla o acesso de leitura e escrita na placa, assim como o envio de comandos para os demais circuitos integrados, foi formado com 3 portas *Not OU* (74LS02) [TEXAS INSTRUMENTS] e o circuito integrado 74LS688 [TEXAS INSTRUMENTS] (Comparador octal).

Ao invés de se implementar uma lógica complexa, o circuito 74LS688, permite descobrir quando é acessado o endereço da placa, pré-programado através do DIP-SWITCH. Desse modo, é possível alterar o endereço da placa quando o mesmo se encontra em uso por outros periféricos do compudator.

Os componentes de apoio (resistências, capacitores) foram colocados conforme sugerido nos Data-Sheets dos circuitos integrados.

O circuito elétrico da placa está repesentado no [Desenho 1 - anexo].

Foi estudado uma configuração alternativa para a placa, com os sample/hold antes do multiplexador, para melhor isolamento dos sinais e maior velocidade de aquisição, sem atraso entre um sinal e outro. [Desenho 2 - anexo]

O protótipo da placa [Figura 10] foi montado em Wire-wrap em uma proto-board compatível com IBM-PC de 8 bits. Este tipo de montagem não é recomendado para montagens de precisão por poder sofrer interferências.

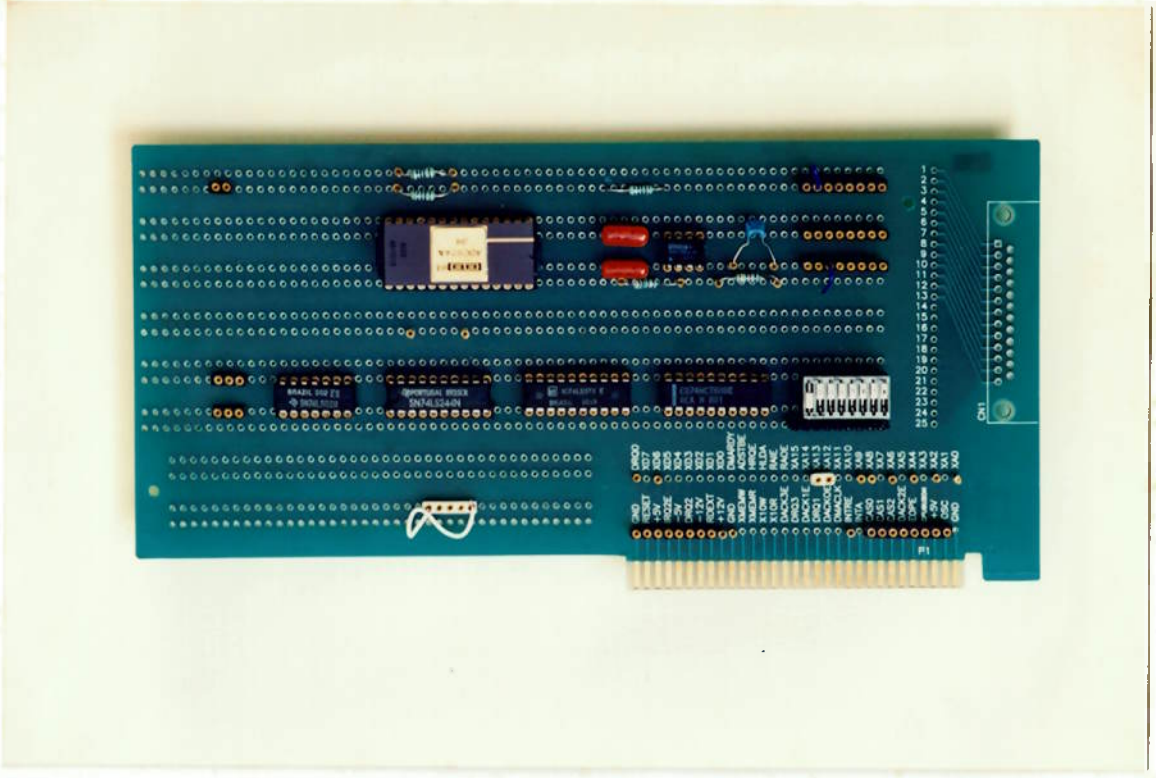


Figura 10 - Proto-Board

A proto-board se encaixa em um slot padrão ISA (Industry Standard Architecture) de 8 ou 16 bits [Figura 11]. A transferência de dados e comandos entre a placa e o computador se dá em blocos de 8 bits.

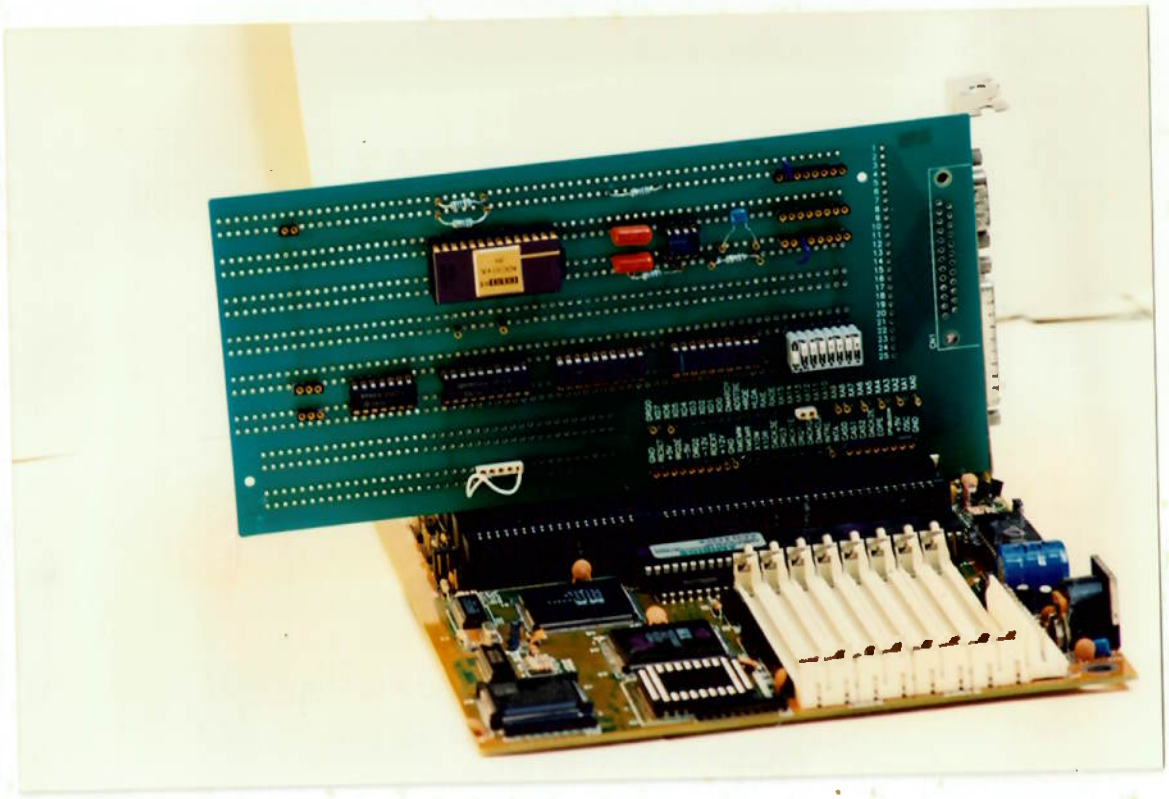


Figura 11 - Placa encaixada no Slot padrão ISA

3.4 - TESTE DO PROTÓTIPO

A placa aquisita sinais na faixa de -5 a +5V.

Um programa escrito na linguagem Turbo Pascal 6.0 é utilizado para testar o funcionamento da placa. No lugar da régua linear e do transdutor de pressão, é utilizado um gerador de sinais.

Por medida de segurança, o sinal máximo é de +5V, por ser utilizada a fonte do próprio computador, onde a placa está instalada.

CAPÍTULO 4 - CONCLUSÕES

Para aquisitar os sinais e controlar a placa, é possível manter o circuito eletrônico simples, investindo apenas na sofisticação do software. Pode ser introduzido o tratamento dos sinais e redução de ruídos.

Mas o maior número de funções adicionadas por software requer maior capacidade no computador que controla a placa, assim como dedicação total do equipamento a este controle.

BIBLIOGRAFIA

- SOUZA, S.A. "ENSAIOS MECÂNICOS DE MATERIAIS METÁLICOS", EDITORA EDGARD BLÜCHER LTDA, SÃO PAULO, BRASIL, 1974

- DIETER, G.E. "MECHANICAL METALLURGY", MCGRAW-HILL, LONDON, U.K., 1988.

- MADUREIRA, O.M. "PMC-475 - METODOLOGIA DO PROJETO", EPUSP, 1993.

- BURR-BROWN "BURR-BROWN IC DATA BOOK".

- TEXAS INSTRUMENTS "TTL DATA BOOK".

- MOTOROLA "DATA BOOK".

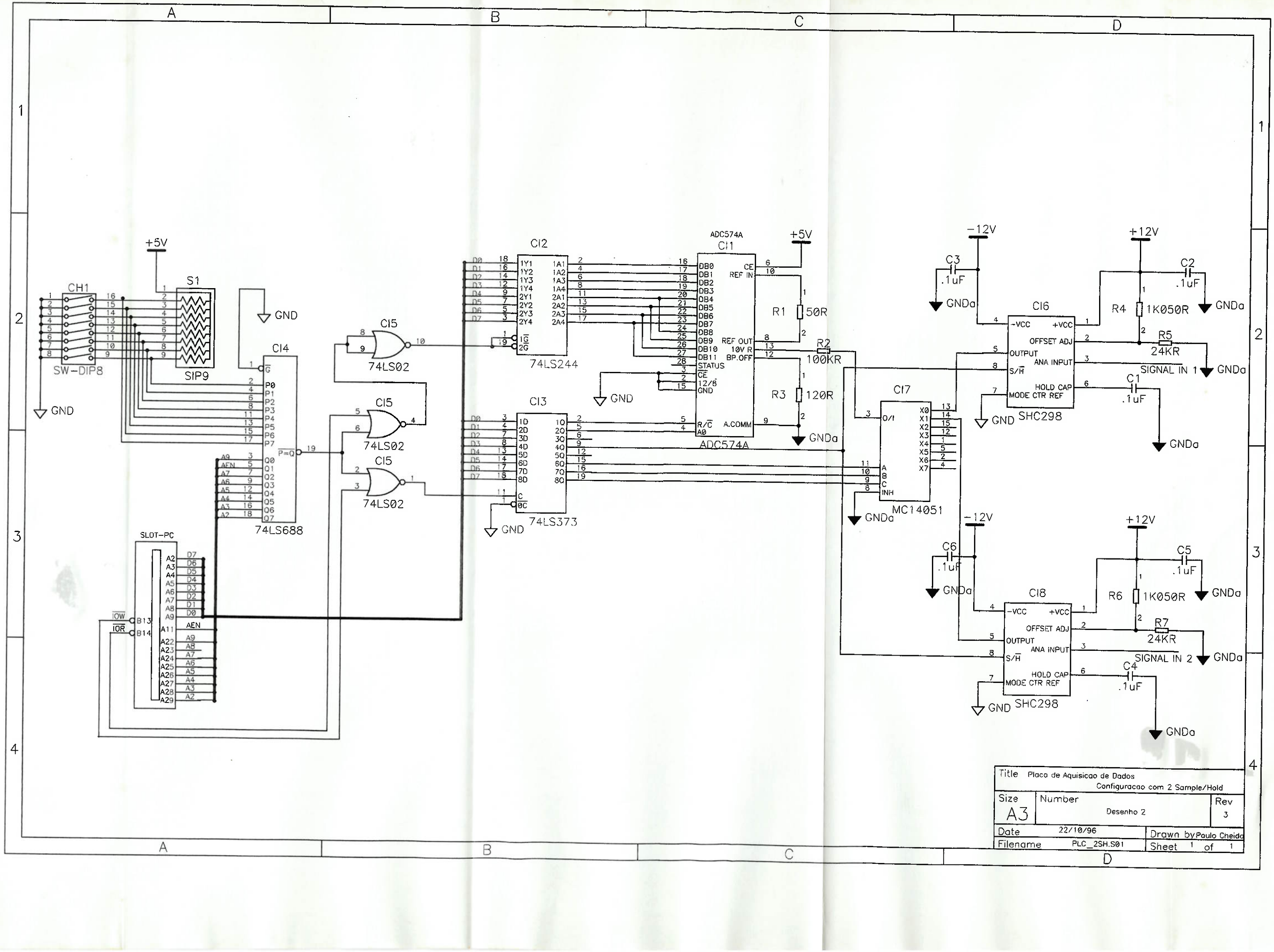
- DIAS JÚNIOR, W.A., "MICROPROCESSADORES 8086/8808: HARDWARE & SOFTWARE", EDITORA MCGRAW-HILL LTDA., SÃO PAULO, BRASIL, 1990.

- SHIMADZU "SHIMADZU UNIVERSAL TESTING MACHINES - TYPE RH - INSTRUCTION FOR USE.", SHIMADZU SEISAKUSO LTD, KYOTO, JAPAN.

Anexo 1

Desenhos dos circuitos da placa

Title	Placa de Aquisicao de Dados Configuracao com 1 Sample/Hold	
Size A3	Number Desenho 1	Rev 7
Date 21/10/96		Drawn by Pauto Cheida
Filename PLC.S01		Sheet 1 of 1


A
B
C
D
1
2
3
4
+5V
CH1
SW-DIP8
S1
SIP9
GND
CI4
74LS688
P=Q
CI5
74LS02
CI2
74LS244
CI3
74LS373
ADC574A
CI1
REF IN
REF OUT
10V R
BP.OFF
STATUS
12/8
A.COMM
R1
50R
R2
100KR
R3
120R
GNDa
CI7
MC14051
-12V
+12V
C3
.1uF
C2
C1
C6
C5
C4
CI6
CI8
SHC298
R4
1K050R
R5
24KR
R6
R7
OFFSET ADJ
OUTPUT
ANA INPUT
S/H
HOLD CAP
MODE CTR REF
SIGNAL IN 1
SIGNAL IN 2
SLOT-PC
IOW
IOR
AEN
Title Placa de Aquisicao de Dados
Configuracao com 2 Sample/Hold
Size A3
Number Desenho 2
Rev 3
Date 22/10/96
Drawn by Paulo Cheida
Filename PLC_2SH.S01
Sheet 1 of 1

A
B
C
D
1
2
3
4
+5V
CH1
S1
SW-DIP8
SIP9
GND
CI4
74LS688
CI5
74LS02
CI2
74LS244
CI3
74LS373
ADC574A
CI1
+5V
-12V
+12V
C3
.1uF
C2
.1uF
GNDa
CI6
SHC298
R1
50R
R2
100KR
R3
120R
R4
1K050R
R5
24KR
C1
.1uF
SIGNAL IN
SLOT-PC
IOW
IOR
Title Placa de Aquisicao de Dados
Configuracao sem Multiplexador
Size A3
Number Desenho 3
Rev 2
Date 23/10/96
Drawn by Paulo Cheida
Filename PLC_NOMX.S01
Sheet 1 of 1

Anexo 2

Programa de teste da placa

```
program Placa;
uses CRT,DOS;
const Porta : integer = $0300;

function le_placa1 : integer;   { Conversao de 8 bits }
var temp,i : integer;
begin
     port[Porta] := $0b;    { Sample }
     port[Porta] := $03;    { Hold   }
     port[Porta] := $02;    { Inicia Conversao de 8 bits }
     port[Porta] := $01;    { Permite a saida dos 8 bits mais significativos }
     for i := 1 to 10 do ;
     temp := Port[Porta];   { Leitura dos bits }
     le_placa1 := temp;
end;

function le_placa10 : integer;  { Conversao de 8 bits }
var temp,i : integer;
begin
     port[Porta] := $0b;    { Sample }
     port[Porta] := $03;    { Hold   }
     port[Porta] := $00;    { Inicia Conversao de 8 bits }
     port[Porta] := $01;    { Permite a saida dos 8 bits mais significativos }
     for i := 1 to 10 do ;
     temp := Port[Porta];   { Leitura dos bits }
     port[Porta] := $03;    { Permite a saida dos 4 bits menos significativos }
     temp := (temp shl 8) + port[Porta];
     le_placa10 := (temp shr 4);
end;

function le_placa20 : integer;  { Conversao de 12 bits }
var temp,i : integer;
begin
     port[Porta] := $2b;    { Sample }
     port[Porta] := $23;    { Hold   }
     port[Porta] := $20;    { Inicia Conversao de 8 bits }
     port[Porta] := $21;    { Permite a saida dos 8 bits mais significativos }
     for i := 1 to 10 do ;
     temp := Port[Porta];   { Leitura dos bits }
     port[Porta] := $23;    { Permite a saida dos 4 bits menos significativos }
     temp := (temp shl 8) + port[Porta];
     le_placa20 := (temp shr 4);
end;

var i : integer;

begin

clrscr;

while not keypressed do    { Repete ate que uma tecla seja pressionada }
begin
     write(le_placa10:5);  { Escreve no video o valor amostrado pela placa }
     for i := 1 to 10 do;
end;

end.
```

Anexo 3

Data sheets dos circuitos integrados

BURR-BROWN®

ADC574A

Microprocessor-Compatible ANALOG-TO-DIGITAL CONVERTER

FEATURES

- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE, CLOCK, AND 8-, 12-, OR 16-BIT MICROPROCESSOR BUS INTERFACE
- IMPROVED PERFORMANCE SECOND SOURCE FOR 574A-TYPE A/D CONVERTERS
  - Conversion Time: 25μs max
  - Bus Access Time: 150ns max
  - A_0 Input: Bus Contention During Read Operation Eliminated
- DUAL IN-LINE PLASTIC AND HERMETIC CERAMIC
- FULLY SPECIFIED FOR OPERATION ON ±12V OR ±15V SUPPLIES
- NO MISSING CODES OVER TEMPERATURE:
  - 0°C to +75°C: ADC574AJH, KH, JP, KP Grades
  - −55°C to +125°C: ADC574ASH, TH Grades

DESCRIPTION

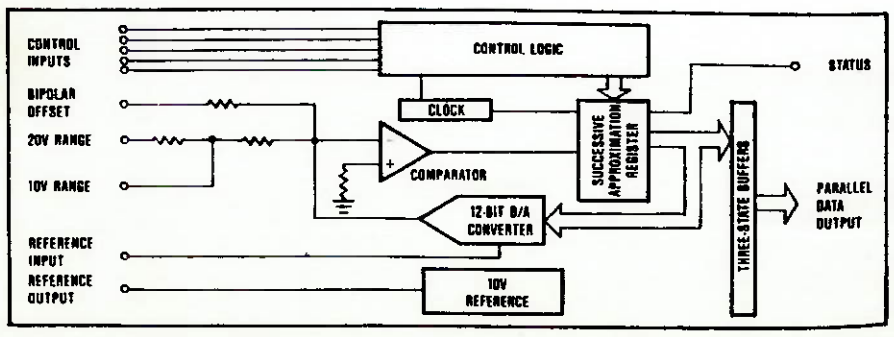
The ADC574A is a 12-bit successive approximation analog-to-digital converter, utilizing state of the art CMOS and laser-trimmed bipolar die custom-designed for freedom from latch-up and for optimum AC performance. It is complete with a self-contained +10V reference, internal clock, digital interface for microprocessor control, and three-state outputs.

The reference circuit, containing a buried zener, is laser-trimmed for minimum temperature coefficient. The clock oscillator is current-controlled for excellent stability over temperature. Full-scale and offset errors may be externally trimmed to zero. Internal scaling resistors are provided for the selection of analog input signal ranges of 0V to +10V, 0V to +20V, ±5V, and ±10V.

The converter may be externally programmed to provide 8- or 12-bit resolution. The conversion time for 12 bits is factory set for 25μs maximum.

Output data are available in a parallel format from TTL-compatible three-state output buffers. Output data are coded in straight binary for unipolar input signals and bipolar offset binary for bipolar input signals.

The ADC574A, available in both industrial and military temperature ranges, requires supply voltages of +5V and ±12V or ±15V. It is packaged in a 28-pin plastic DIP, or hermetic side-brazed ceramic DIP.



International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 06-8401

PDS-550C

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V, V_{LOGIC} = +5V unless otherwise specified.

MODEL	ADC574AJP, ADC574AJH, ADC574ASH			ADC574AKP, ADC574AKH, ADC574ATH			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION			12			•	Bits
INPUTS							
ANALOG							
Voltage Ranges: Unipolar		0 to +10, 0 to +20			•		V
Bipolar		±5, ±10			•		V
Impedance: 0 to +10V, ±5V	4.7	5	5.3	•	•	•	kΩ
±10V, 0V to +20V	9.4	10	10.6	•	•	•	kΩ
DIGITAL (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/8)							
Over Temperature Range							
Voltages: Logic 1	+2.0		+5.5	•		•	V
Logic 0	−0.5		+0.8	•		•	V
Current	−5	0.1	+5	•		•	μA
Capacitance		5			•		pF
TRANSFER CHARACTERISTICS							
ACCURACY							
@+25°C							
Linearity Error			±1			±1/2	LSB
Unipolar Offset Error (adjustable to zero)			±2			•	LSB
Bipolar Offset Error (adjustable to zero)			±10			±4	LSB
Full-Scale Calibration Error[11] (adjustable to zero)			±0.25			•	% of FS[12]
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
Inherent Quantization Error		±1/2			•		LSB
T_{MIN} to T_{MAX}							
Linearity Error: J, K Grades			±1			±1/2	LSB
S, T Grades			±1			±1/2	LSB
Full-Scale Calibration Error							
Without Initial Adjustment[11]: J, K Grades			±0.47			±0.37	% of FS
S, T Grades			±0.75			±0.5	% of FS
Adjusted to zero at +25°C: J, K Grades			±0.22			±0.12	% of FS
S, T Grades			±0.5			±0.25	% of FS
No Missing Codes Resolution (Diff. Linearity)	11			12			Bits
TEMPERATURE COEFFICIENTS (T_{MIN} to T_{MAX})[13]							
Unipolar Offset: J, K Grades			±10			±6	ppm/°C
S, T Grades			±5			±2.5	ppm/°C
Max Change: All Grades			±2			±1	LSB
Bipolar Offset: All Grades			±10			±5	ppm/°C
Max Change: J, K Grades			±2			±1	LSB
S, T Grades			±4			±2	LSB
Full-Scale Calibration: J, K Grades			±45			±25	ppm/°C
S, T Grades			±50			±25	ppm/°C
Max Change: J, K Grades			±9			±5	LSB
S, T Grades			±20			±10	LSB
POWER SUPPLY SENSITIVITY							
Change in Full-Scale Calibration							
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V			±2			±1	LSB
−16.5V < V_{EE} < −13.5V or −12.6V < V_{EE} < −11.4V			±2			±1	LSB
+4.5V < V_{LOGIC} < +5.5V			±1/2			•	LSB
CONVERSION TIME[14]							
8-Bit Cycle	10	13	17	•	•	•	μs
12-Bit Cycle	15	20	25	•	•	•	μs
OUTPUTS							
DIGITAL (DB_{11} — DB_0, STATUS)							
Over Temperature Range)							
Output Codes: Unipolar			Unipolar Straight Binary (USB)				
Bipolar			Bipolar Offset Binary (BOB)				
Logic Levels: Logic 0 (I_{SINK} = 1.6mA)			+0.4			•	V
Logic 1 (I_{SOURCE} = 500μA)	+2.4			•			V
Leakage, Data Bits Only, High-Z State	−5	0.1	+5	•	•	•	μA
Capacitance		5			•		pF
INTERNAL REFERENCE VOLTAGE							
Voltage	+9.9	+10.0	+10.1	•	•	•	V
Source Current Available for External Loads[15]	2.0			•			mA

	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER SUPPLY REQUIREMENTS							
Voltage V_{CC}	+11.4		+16.5	•		•	V
V_{EE}	−11.4		−16.5	•		•	V
V_{LOGIC}	+4.5		+5.5	•		•	V
Current I_{CC}		3.5	5		•	•	mA
I_{EE}		15	20		•	•	mA
I_{LOGIC}		9	15		•	•	mA
Power Dissipation (±15V Supplies)		325	450		•	•	mW
TEMPERATURE RANGE (Ambient T_{MIN}, T_{MAX})							
Specification J, K Grades	0		+75	•		•	°C
S, T Grades	−55		+125	•		•	°C
Storage	−65		+150	•		•	°C

*Same specification as ADC574AJP, AJH, ASH

NOTES: (1) With fixed 50Ω resistor from REF OUT to REF IN. This parameter is also adjustable to zero at +25°C (see Optional External Full Scale and Offset Adjustments section). (2) FS in this specification table means Full Scale Range. That is, for a ±10V input range, FS means 20V; for a 0 to +10V range, FS means 10V. The term Full Scale for these specifications instead of Full-Scale Range is used to be consistent with other vendors' 574 and 574A type specification tables. (3) Using internal reference. (4) See Controlling the ADC574A section for detailed information concerning digital timing. (5) External loading must be constant during conversion. The reference output requires no buffer amplifier with either ±12V or ±15V power supplies.

ORDERING INFORMATION

Model	Package (DIP)	Temperature Range	Linearity Error, max (T_{MIN} to T_{MAX})
ADC574AJP	Plastic	0°C to +75°C	±1LSB
ADC574AKP	Plastic	0°C to +75°C	±1/2LSB
ADC574AJH	Ceramic	0°C to +75°C	±1LSB
ADC574AKH	Ceramic	0°C to +75°C	±1/2LSB
ADC574ASH	Ceramic	−55°C to +125°C	±1LSB
ADC574ATH	Ceramic	−55°C to +125°C	±1/2LSB
BURN-IN SCREENING OPTION See text for details			
Model	**Package (DIP)**	**Temperature Range**	**Burn-In Temp. (160 Hours)[1]**
ADC574AJP-BI	Plastic	0°C to +75°C	+85°C
ADC574AKP-BI	Plastic	0°C to +75°C	+85°C
ADC574AJH-BI	Ceramic	0°C to +75°C	+125°C
ADC574AKH-BI	Ceramic	0°C to +75°C	+125°C
ADC574ASH-BI	Ceramic	−55°C to +125°C	+125°C
ADC574ATH-BI	Ceramic	−55°C to +125°C	+125°C

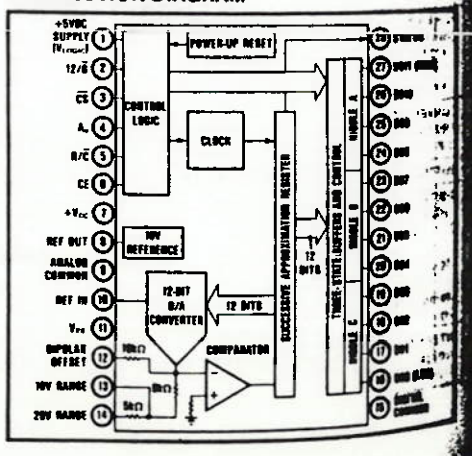
NOTE: (1) Or equivalent combination of time and temperature.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common	0 to +16.5V
V_{EE} to Digital Common	0 to −16.5V
V_{LOGIC} to Digital Common	0 to +7V
Analog Common to Digital Common	±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/8, R/$\overline{C}$) to Digital Common	0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common	+16.5V
$20V_{IN}$ to Analog Common	±24V
REF OUT	Indefinite Short to Common, Momentary Short to V_{CC}
Max Junction Temperature	+165°C
Power Dissipation	1000mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA} Ceramic	50°C/W
Plastic	100°C/W

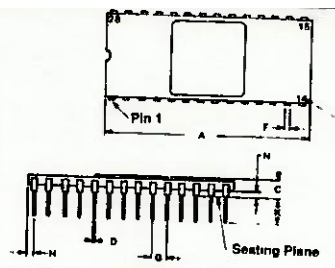
CAUTION: These devices are sensitive to electrostatic discharge. Appropriate I.C. handling procedures should be followed.

CONNECTION DIAGRAM



J Package [Ceramic]

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.386	1.414	35.20	35.92
C	.108	.186	2.74	4.22
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.036	.064	0.91	1.63
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	—	10°	—	10°
N	.025	.060	0.64	1.52



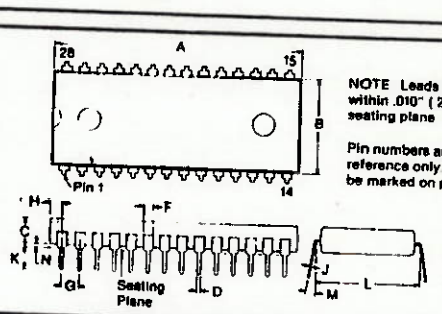
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

CASE: Ceramic, hermetic
WEIGHT: 4.8 grams (0.17 oz.)

P Package [Plastic]

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.350	1.450	34.29	36.83
B	.520	.575	13.21	14.61
C	.189	.224	4.80	5.70
D	.015	.023	0.38	0.58
F	.043	.062	1.09	1.57
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.150	2.54	3.81
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.040	0.46	1.02



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers are shown for reference only. Numbers may not be marked on package.

CASE: Plastic
WEIGHT: 4.3 grams (0.15oz.)

DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of actual code transition values from the ideal transition values. Ideal transition values lie on a line drawn through zero (or minus full scale for bipolar operation) and plus full scale. The zero value is located at an analog input value 1/2LSB before the first code transition (000_H to 001_H). The full-scale value is located at an analog value 3/2LSB beyond the last code transition (FFE_H to FFF_H) (see Figure 1).

Thus, for a converter connected for bipolar operation and with a full-scale range (or span) of 20V (±10V), the zero value of −10V is 2.44mV below the first code transition (000_H to 001_H at −9.99756V) and the plus full-scale value of +10V is 7.32mV above the last code transition (FFE_H to FFF_H at +9.99268) (see Table I).

NO MISSING CODES (DIFFERENTIAL LINEARITY ERROR)

A specification which guarantees no missing codes requires that every code combination appear in a monotonically-increasing sequence as the analog input is increased throughout the range. Thus, every input code width (quantum) must have a finite width. If an input quantum has a value of zero (a differential linearity error of −1LSB), a missing code will occur.

ADC574AKP, KH, and TH grades are guaranteed to have no missing codes to 12-bit resolution over their respective specification temperature ranges.

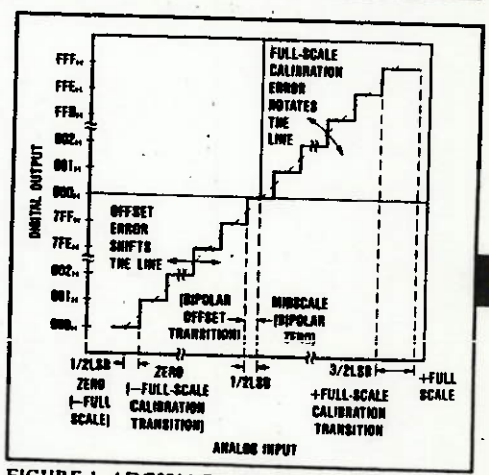


FIGURE 1. ADC574A Transfer Characteristic Terminology.

UNIPOLAR OFFSET ERROR

An ADC574A connected for unipolar operation has an analog input range of 0V to plus full scale. The first output code transition should occur at an analog input value 1/2LSB above 0V. Unipolar offset error is defined as the deviation of the actual transition value from the ideal value. The unipolar offset temperature coefficient specifies the change of this transition value versus a change in ambient temperature.

Binary (BIN) Output	Input Voltage Range and LSB Values				
Analog Input Voltage Range	Defined As	±10V	±5V	0 to +10V	0 to +20V
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{10V}{2^n}$	$\frac{20V}{2^n}$
	n = 8	78.13mV	39.06mV	39.06mV	78.13mV
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
Output Transition Values					
FFE_H to FFF_H	+ Full-Scale Calibration	+10V – 3/2LSB	+5V – 3/2LSB	+10V – 3/2LSB	+10V – 3/2LSB
$7FF_H$ to 800_H	Midscale Calibration (Bipolar Offset)	0 – 1/2LSB	0 – 1/2LSB	+5V – 1/2LSB	±10V – 1/2LSB
000_H to 001_H	Zero Calibration (– Full Scale Calibration)	–10V + 1/2LSB	–5V + 1/2LSB	0 to + 1/2LSB	0 to +1/2LSB

BIPOLAR OFFSET ERROR

A/D converter specifications have historically defined bipolar offset as the first transition value above the minus full-scale value. The ADC574A specification, however, follows the terminology defined for the 574 converter several years ago. Thus, bipolar offset is located near the midscale value of 0V (bipolar zero) at the output code transition $7FF_H$ to 800_H.

Bipolar offset error for the ADC574A is defined as the deviation of the actual transition value from the ideal transition value located 1/2LSB below 0V. The bipolar offset temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

FULL SCALE CALIBRATION ERROR

The last output code transition (FFE_H to FFF_H) occurs for an analog input value 3/2LSB below the nominal full-scale value. The full scale calibration error is the deviation of the actual analog value at the last transition point from the ideal value. The full-scale calibration temperature coefficient specifies the maximum change of the code transition value versus a change in ambient temperature.

POWER SUPPLY SENSITIVITY

Electrical specifications for the ADC574A assume the application of the rated power supply voltages of +5V and ±12V or ±15V. The major effect of power supply voltage deviations from the rated values will be a small change in the full-scale calibration value. This change, of course, results in a proportional change in all code transition values (i.e. a gain error). The specification describes the maximum change in the full-scale calibration value from the initial value for a change in each power supply voltage.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset and bipolar offset specify the maximum change from the +25°C value to the value at T_{MIN} or T_{MAX}.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters have an inherent quantization error of ±1/2LSB. This error is a fundamental property of the quantization process and cannot be eliminated.

CODE WIDTH (QUANTUM)

Code width, or quantum, is defined as the range of analog input values for which a given output code will occur. The ideal code width is 1LSB.

INSTALLATION

LAYOUT PRECAUTIONS

Analog (pin 9) and digital (pin 15) commons are not connected together internally in the ADC574A, but should be connected together as close to the unit as possible and to an analog common ground plane beneath the converter on the component side of the board. In addition, a wide conductor pattern should run directly from pin 9 to the analog supply common, and a separate wide conductor pattern from pin 15 to the digital supply common. Analog common (pin 9) typically carries ±8mA.

If the single-point system common cannot be established directly at the converter, pin 9 and pin 15 should still be connected together at the converter; a single wide conductor pattern then connects these two pins to the system common. In either case, the common return of the analog input signal should be referenced to pin 9 of the ADC. This prevents any voltage drops that might occur in the power supply common returns from appearing in series with the input signal.

Coupling between analog input and digital lines should be minimized by careful layout. For instance, if the lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated from each other by a pattern connected to common.

If external full scale and offset potentiometers are used, the potentiometers and associated resistors should be located as close to the ADC574A as possible. If no adjustments are used, the fixed resistors should likewise be as close as possible.

POWER SUPPLY DECOUPLING

Logic and analog power supplies should be bypassed with 10μF tantalum type capacitors located close to the converter to obtain noise-free operation. Noise on these power supply lines can degrade the converter's performance. Noise and spikes from a switching power supply are especially troublesome.

signal source supplying the analog input signal to ADC574A will be driving into a nominal DC input edance of either 5kΩ or 10kΩ. However, the output edance of the driving source should be very low, such the output impedance provided by a wideband, fast- ling operational amplifier. Transients in A/D input rent are caused by the changes in output current of internal D/A converter as it tests the various bits. output voltage of the driving source must remain tant while furnishing these fast current changes. If application requires a sample/hold, select a sample/ d with sufficient bandwidth to preserve the accuracy use a separate wideband buffer amplifier to lower the put impedance.

NGE CONNECTIONS

ADC574A offers four standard input ranges: 0V to V, 0V to +20V, ±5V, and ±10V. If a 10V input range required, the analog input signal should be connected pin 13 of the converter. A signal requiring a 20V range connected to pin 14. In either case the offset pin of the e is left unconnected. Full-scale and offset adjust- t are described below.

operate the converter with a 10.24V (2.5mV LSB) or V (5mV LSB) input range, insert a 120Ω 1% metal- resistor in series with pin 13 for the 10.24V range, or Ω 1% metal-film resistor in series with pin 14 for the V range. Offset and gain adjustments are still formed as described below. However, you must recal- full-scale adjustment voltages proportionately. A d metal-film resistor can be used because the input pedance of the ADC574A is trimmed to less than ±6% the nominal value.

CALIBRATION

TIONAL EXTERNAL FULL-SCALE AND FSET ADJUSTMENTS

set and full-scale errors may be trimmed to zero using nal offset and full-scale trim potentiometers con- ted to the ADC574A as shown in Figures 2 and 3 for olar and bipolar operation.

LIBRATION PROCEDURE— IPOLAR RANGES

adjustment of unipolar offset and full scale is not uired, replace R_2 with a 50Ω, 1% metal film resistor connect pin 12 to pin 9, omitting the adjustment work.

adjustment is required, connect the converter as wn in Figure 2. Sweep the input through the end- nt transition voltage (0V + 1/2LSB; +1.22mV for the V range; +2.44mV for the 20V range) that causes the put code to be DB0 ON (high). Adjust potentiometer until DB0 is alternately toggling ON and OFF with other bits OFF. Then adjust full scale by applying an put voltage of nominal full-scale value minus 3/2LSB, value which should cause all bits to be ON. This the 20V range. Adjust potentiometer R_2 until bits DB1—DB11 are ON and DB0 is toggling ON and OFF.

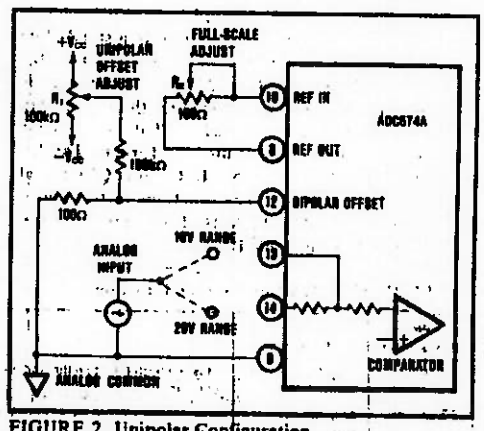


FIGURE 2. Unipolar Configuration.

CALIBRATION PROCEDURE—BIPOLAR RANGES

If external adjustments of full-scale and bipolar offset are not required, the potentiometers may be replaced by 50Ω, 1% metal film resistors.

If adjustments are required, connect the converter as shown in Figure 3. The calibration procedure is similar to that described above for unipolar operation, except that the offset adjustment is performed with an input voltage which is 1/2LSB above the minus full-scale value (–4.9988V for the ±5V range, –9.9976V for the ±10V range). Adjust R_1 for DB0 to toggle ON and OFF with all other bits OFF. To adjust full-scale, apply a DC input signal which is 3/2LSB below the nominal plus full-scale value (+4.9963V for ±5V range, +9.9927V for ±10V range) and adjust R_2 for DB0 to toggle ON and OFF with all other bits ON.

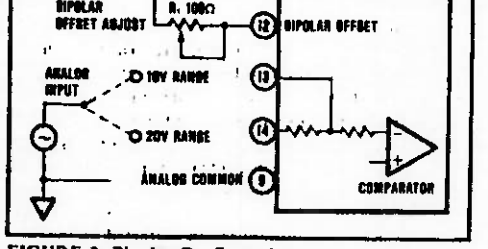


FIGURE 3. Bipolar Configuration.

The Burr-Brown ADC574A can be easily interfaced to most microprocessor systems and other digital systems. The microprocessor may take full control of each conversion, or the converter may operate in a stand-alone mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the ouptut data when ready choosing either 12 bits all at once, or 8 bits followed by 4 bits in a left-justified format. The five control inputs (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$, and CE) are all TTL CMOS-compatible. The functions of the control inputs are described in Table II. The control function truth table is listed in Table III.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeros

TABLE II. ADC574A Control Line Functions.

Pin Designation	Definition	Function
CE (Pin 6)	Chip Enable (active high)	Must be high ("1") to either initiate a conversion or read output data. 0-1 edge may be used to initiate a conversion
$\overline{CS}$ (Pin 3)	Chip Select (active low)	Must be low ("0") to either initiate a conversion or read output data. 1-0 edge may be used to initiate a conversion
R/$\overline{C}$ (Pin 5)	Read/Convert ("1" = read) ("0" = convert)	Must be low ("0") to initiate either 8 or 12-bit conversions. 1-0 edge may be used to initiate a conversion. Must be high ("1") to read output data. 0-1 edge may be used to initiate a read operation
A_0 (Pin 4)	Byte Address Short Cycle	In the start-convert mode, A_0 selects 8-bit (A_0 = "1") or 12-bit (A_0 = "0") conversion mode. When reading output data in two 8-bit bytes, A_0 = "0" accesses 8 MSBs (high byte) and A_0 = "1" accesses 4 LSBs and trailing "0s" (low byte)
12/$\overline{8}$ (Pin 2)	Data Mode Select ("1" = 12 bits) ("0" = 8 bits)	When reading output data, 12/$\overline{8}$ = "1" enables all 12 output bits simultaneously. 12/$\overline{8}$ = "0" will enable the MSB's or LSB's as determined by the A_0 line

STAND-ALONE OPERATION

For stand-alone operation, control of the converter is accomplished by a single control line connected to R/$\overline{C}$. In this mode $\overline{CS}$ and A_0 are connected to digital common and CE and 12/$\overline{8}$ are connected to V_{LOGIC} (+5V). The output data are presented as 12-bit words. The stand-alone mode is used in systems containing dedicated input ports which do not require full bus interface capability.

Conversion is initiated by a high-to-low transition of R/$\overline{C}$. The three-state data output buffers are enabled when R/$\overline{C}$ is high and STATUS is low. Thus, there are two possible modes of operation; conversion can be initiated with either positive or negative pulses. In either case the R/$\overline{C}$ pulse must remain low for a minimum of 50ns.

Figure 4 illustrates timing when conversion is initiated by an R/$\overline{C}$ pulse which goes low and returns to the high state during the conversion. In this case, the three-state outputs go to the high-impedance state in response to the falling edge of R/$\overline{C}$ and are enabled for external access of the data after completion of the conversion. Figure 5 illustrates the timing when conversion is initiated by a positive R/$\overline{C}$ pulse. In this mode the ouptut data from the previous conversion is enabled during the positive portion of R/$\overline{C}$. A new conversion is started on the falling edge of R/$\overline{C}$, and the three-state outputs return to the high-impedance state until the next occurrence of a high R/$\overline{C}$ pulse. Table IV lists timing specifications for stand-alone operation.

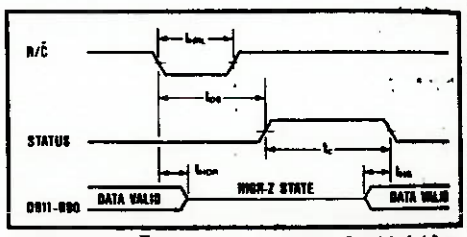


FIGURE 4. R/$\overline{C}$ Pulse Low — Outputs Enabled After Conversion.

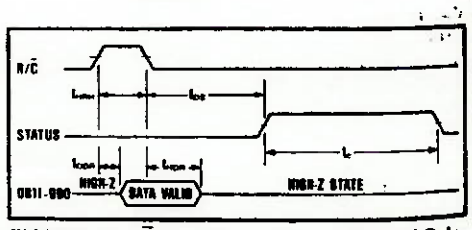


FIGURE 5. R/$\overline{C}$ Pulse High — Outputs Enabled Only While R/$\overline{C}$ Is High.

Symbol	Parameter	Min	Typ	Max	Units
t_{HR}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{SR}	STS Delay from R/$\overline{C}$			200	ns
t_{DR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{DS}	STS Delay After Data Valid	300	400	1000	ns
t_{HD}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

FULLY CONTROLLED OPERATION

Conversion Length

Conversion length (8-bit or 12-bit) is determined by the state of the A_0 input, which is latched upon receipt of a conversion start transition (described below). If A_0 is latched high, the conversion continues for 8 bits. The full 12-bit conversion will occur if A_0 is low. If all 12 bits are read following an 8-bit conversion, the 3LSBs (DB0–DB2) will be low (logic 0) and DB3 will be high (logic 1). A_0 is latched because it is also involved in enabling the output buffers. No other control inputs are latched.

CONVERSION START

The converter is commanded to initiate conversion by a transition occurring on any of three logic inputs (CE, $\overline{CS}$, and R/$\overline{C}$) as shown in Table III. Conversion is initiated by the last of the three to reach the required state and thus all three may be dynamically controlled. If necessary, all three may change states simultaneously, and the nominal delay time is the same regardless of which input actually starts conversion. If it is desired that a particular input establish the actual start of conversion, the other two should be stable a minimum of 50ns prior to the transition of that input. Timing relationships for start of conversion timing are illustrated in Figure 6. The specifications for timing are contained in Table V.

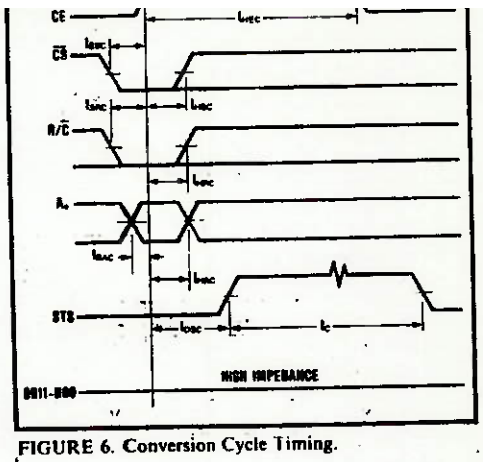


FIGURE 6. Conversion Cycle Timing.

The STATUS output indicates the current state of the converter by being in a high state only during conversion. During this time the three state output buffers remain in a high-impedance state, and therefore data cannot be read during conversion. During this period additional transitions of the three digital inputs which control conversion will be ignored, so that conversion cannot be prematurely terminated or restarted. However, if A_0 changes state after the beginning of conversion, any additional start conversion transition will latch the new state of A_0, possibly resulting in an incorrect conversion length (8 bits vs 12 bits) for that conversion.

TABLE V. Timing Specifications.

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS delay from CE		60	200	ns
t_{HEC}	CE Pulse width	50	30		ns
t_{SSC}	$\overline{CS}$ to CE setup	50	20		ns
t_{SSC}	$\overline{CS}$ low during CE high	50	20		ns
t_{SRC}	R/$\overline{C}$ to CE setup	50	0		ns
t_{HRC}	R/$\overline{C}$ low during CE high	50	20		ns
t_{SAC}	A_0 to CE setup	0			ns
t_{HAC}	A_0 valid during CE high	50	20		ns
t_C	Conversion time, 12 bit cycle	15	20	25	µs
	8 bit cycle	10	13	17	µs
Read Mode					
t_{DD}	Access time from CE		75	150	ns
t_{HD}	Data valid after CE low	25	35		ns
t_{HL}	Output float delay		100	150	ns
t_{SSR}	$\overline{CS}$ to CE setup	50	0		ns
t_{SRR}	R/$\overline{C}$ to CE setup	0			ns
t_{SAR}	A_0 to CE setup	50	25		ns
t_{HSR}	$\overline{CS}$ valid after CE low	0			ns
t_{HRR}	R/$\overline{C}$ high after CE low	0			ns
t_{HAR}	A_0 valid after CE low	50			ns
t_{HS}	STS delay after data valid	300	400	1000	ns

NOTE: Specifications are at +25°C and measured at 50% level of transitions.

remain in a high-impedance state until the following four logic conditions are simultaneously met: R/$\overline{C}$ high, STATUS low, CE high, and $\overline{CS}$ low. Upon satisfaction of these conditions the data lines are enabled according to the state of inputs 12/$\overline{8}$ and A_0. See Figure 7 and Table V for timing relationships and specifications.

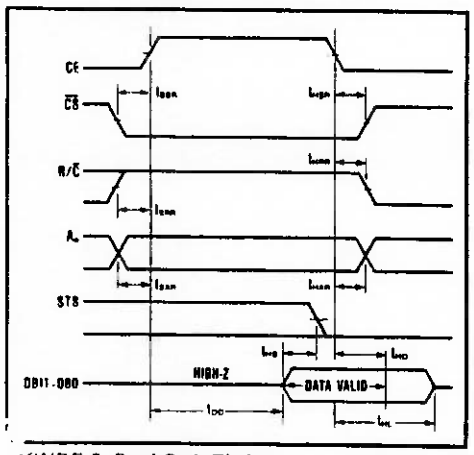


FIGURE 7. Read Cycle Timing.

In most applications the 12/$\overline{8}$ input will be hard-wired in either the high or low condition, although it is fully TTL- and CMOS-compatible and may be actively driven if desired. When 12/$\overline{8}$ is high, all 12 output lines (DB0-DB11) are enabled simultaneously for full data word transfer to a 12-bit or 16-bit bus. In this situation the A_0 state is ignored.

accomplished by the state of A_0 during the read cycle. Connection of the ADC574A to an 8-bit bus for transfer of left-justified data is illustrated in Figure 8. The A_0 input is usually driven by the least significant bit of the address bus, allowing storage of the output data word in two consecutive memory locations.

When A_0 is low, the byte addressed contains the 8MSBs. When A_0 is high, the byte addressed contains the 4LSBs from the conversion followed by four logic zeros which have been forced by the control logic. The left-justified formats of the two 8-bit bytes are shown in Figure 8. The design of the ADC574A guarantees that the A_0 input may be toggled at any time with no damage to the converter; the outputs which are tied together as illustrated in Figure 9 cannot be enabled at the same time.

In the majority of applications the read operation will be attempted only after the conversion is complete and the STATUS output has gone low. In those situations requiring the earliest possible access to the data, the read may be started as much as 1.15µs (t_{DD} max + t_{HS} max) before STATUS goes low. Refer to Figure 7 for these timing relationships.

BURN-IN SCREENING

Burn-in screening is available for both plastic and ceramic package ADC574As. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are 100% electrically tested after burn-in is completed. To order burn-in, add "-BI" to the base model number (e.g., ADC574AKP-BI). See Ordering Information for pricing.

	Word 1								Word 2							
Processor	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Converter	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	0	0	0	0

FIGURE 8. 12-Bit Data Format for 8-Bit Systems.

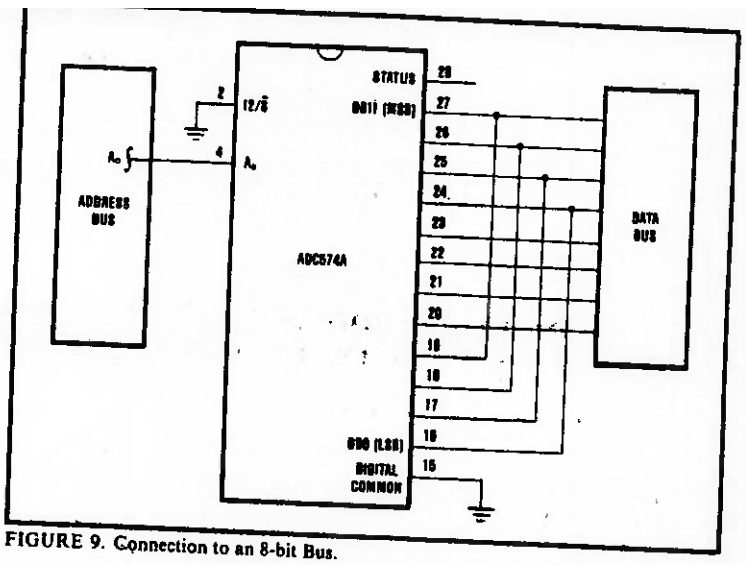
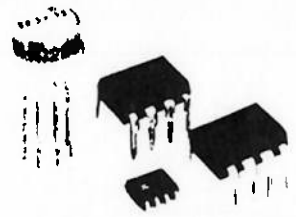


FIGURE 9. Connection to an 8-bit Bus.

BURR-BROWN®

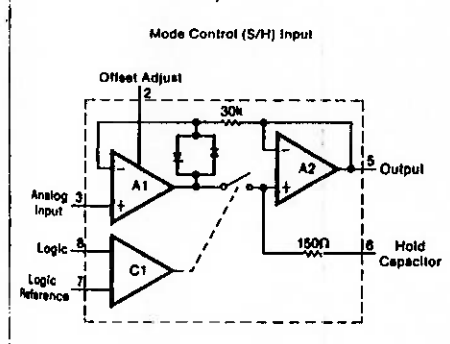


SHC298
SHC298A

Monolithic
SAMPLE/HOLD AMPLIFIER

FEATURES

- 12-BIT THROUGHPUT ACCURACY
- LESS THAN 10μs ACQUISITION TIME
- WIDEBAND NOISE LESS THAN 20μVrms
- RELIABLE MONOLITHIC CONSTRUCTION
- $10^{10}\Omega$ INPUT RESISTANCE
- TTL/CMOS-COMPATIBLE LOGIC INPUT



DESCRIPTION

The SHC298 and SHC298A are high-performance monolithic sample/hold amplifiers featuring high DC accuracy with fast acquisition times and a low droop rate. Dynamic performance and holding performance can be optimized with proper selection of the external holding capacitor. With a 1000pF holding capacitor, 12-bit accuracy can be achieved with a 6μs acquisition time. Droop rates less than 5mV/min are possible with a 1μF holding capacitor.

These sample/holds will operate over a wide supply voltage ranging from ±5V to ±18V with very little change in performance. A separate Offset Adjust pin is used to adjust the offset in either the Sample or the Hold modes. The fully differential logic inputs have low input current, and are compatible with TTL, 5V CMOS, and CMOS logic families.

The SHC298AM is available in a hermetically sealed 8-pin TO-99 package and is specified over a temperature range from −25°C to +85°C. The SHC298JP and SHC298JU are 8-pin plastic DIP and SOIC packaged parts specified over 0°C to +70°C.

The SHC298AJP, specified over 0°C to +70°C, is available in an 8-pin plastic DIP. The SHC298A grade features improved Gain and Offset Error, improved drift over temperature, and faster Acquisition Time.

The SHC298 family is a price-performance bargain. It is well suited for use with several 12-bit A/D converters in data acquisition systems, data distribution systems, and analog delay circuits.

International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734 • Tel.: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

PDS-373C

SPECIFICATIONS

ELECTRICAL

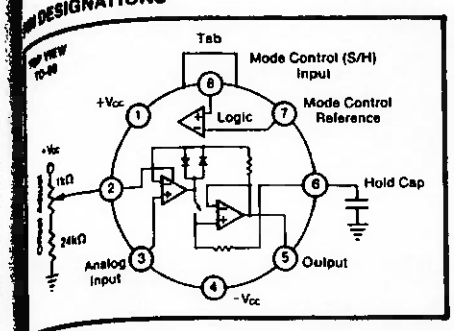
Specifications at T_A = +25°C, ±15V supplies, 1000pF holding capacitor, ±11.5V < V_{IN} < ±11.5, R_L = 10kΩ, Logic Reference Voltage = 0V, and Logic Voltage = 5V unless otherwise noted.

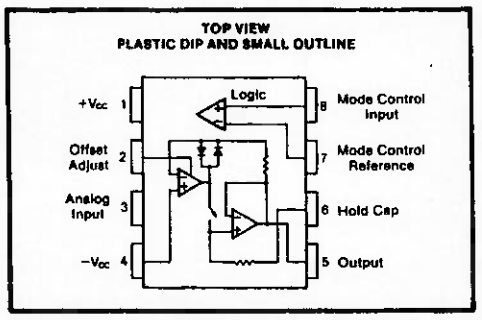
PARAMETER	SHC298AM/JP/JU MIN	SHC298AM/JP/JU TYP	SHC298AM/JP/JU MAX	SHC298AJP MIN	SHC298AJP TYP	SHC298AJP MAX	UNITS
INPUT							
ANALOG INPUT							
Resistance		10^{10}			•		Ω
Bias Current[1]		10	50		•	25	nA
DIGITAL INPUT	Pin 7		Pin8		Circuit State		
Mode Control Truth Table	0V		+2.4V		Sample (Track)		
	0V		+0.8V		Hold		
	+2.4V		+2.8V		Hold		
	+0.8V		+2.8V		Sample (Track)		
Mode Control and Mode Control Reference Input Current			10				μA
Differential Logic Threshold	0.8	1.4	2.4				V
TRANSFER CHARACTERISTICS							
ACCURACY (+25°C)							
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015		•	•	% of 20V
Gain		±1.0			•		V/V
Gain Error		±0.004	±0.010		±0.001	±0.005	%
Input Voltage Offset (adjust to zero)[1]		±2	±7		±1	±2	mV
Droop Rate[1]		±30	±200		•	±100	μV/ms
Charge Offset[2]		±15	±25		•	•	mV
Noise (rms) 10Hz to 100kHz		10	20		•	•	μV
Power Supply Rejection		±25	±100		•	•	μV/V
ACCURACY DRIFT							
Gain Drift		3	4		1	2	ppm/°C
Input Offset Drift		15	70		•	25	μV/°C
Charge Offset Drift C = 1000pF		50	150		•	•	μV/°C
Charge Offset Drift C = 10,000pF		20	50		•	•	μV/°C
Droop Rate at T_A = +85°C		1	10		•	•	mV/ms
DYNAMIC CHARACTERISTICS							
Full Power Bandwidth, C = 1000pF	75	125		•	•		kHz
Full Power Bandwidth C = 10,000pF	10	16		•	•		kHz
Output Slew Rate, C = 1000pF	7	10		•	•		V/μs
Output Slew Rate, C = 10,000pF	1.4	2		•	•		V/μs
Aperture Time, Negative Input Step		200	250		•	•	ns
Positive Input Step		150	200		•	•	ns
Acquisition Time (C = 1000pF) to ±0.01%, 10V step		6	10		•	•	μs
to ±0.01%, 20V step		8	12		•	•	μs
to ±0.1%, 10V step		5	9		4	6	μs
to ±0.1%, 20V step		7	11		•	•	μs
Sample Hold Transient, Peak Amplitude		160			•	•	mV
Settling to 1mV		1.0	1.5		•	•	μs
Feedthrough (Response to 10V Input Step)	—	±0.007	±0.015		±0.004	±0.0075	% of 20V
OUTPUT							
ANALOG OUTPUT							
Voltage Range	±11.5			•			V
Current Range	±2			•			mA
Impedance (in hold mode)		0.5	4		•	•	Ω
POWER SUPPLY							
Rate Voltage	±5.0	±15		•	•	•	VDC
Range			±18				VDC
Current[3]		±4.5	±6.5		•	•	mA

*Same as specifications for SHC298AM/JP/JU

NOTES: (1) These parameters guaranteed over a supply voltage range of ±5V to ±18V. (2) Charge offset is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the charge offset is inversely proportional to hold capacitor value.

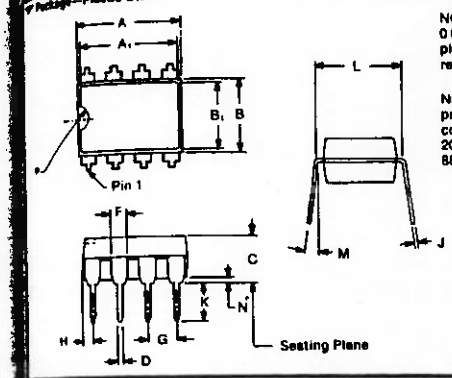
PIN DESIGNATIONS





MECHANICAL

"P" Package—Plastic DIP



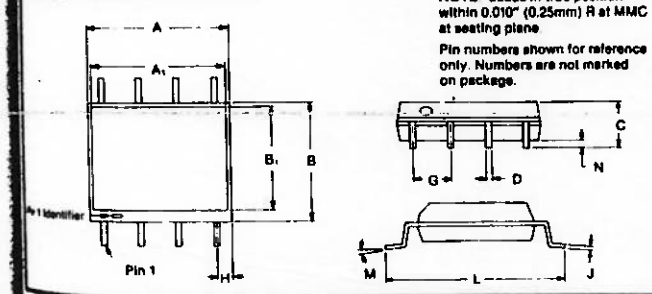
NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only.

Numbers may not be marked on package. Pin material an plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.355	.400	9.03	10.16
A_1	.340	.384	8.64	9.76
B	.230	.290	5.85	7.37
B_1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	100 BASIC		2.54 BASIC	
H	.025	.050	0.64	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

θ_{JA} = 130°C/W

"U" Package—Small Outline Surface Mount



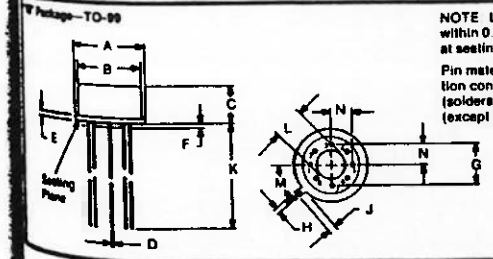
NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers are not marked on package.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.201	4.70	5.11
A_1	.178	.201	4.52	5.11
B	.146	.162	3.71	4.11
B_1	.130	.149	3.30	3.78
C	.064	.145	1.37	3.80
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.018	.026	0.46	0.66
J	.008	.012	0.20	0.30
L	.220	.252	5.59	6.40
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30

θ_{JA} = 150°C/W

"T" Package—TO-99



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).

θ_{JA} = 150°C/W
θ_{JC} = 45°C/W

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Package Limitation)	500mW
Junction Temperature, T_{JMAX}	
AM	125°C
JP, JU	100°C
Operating Temperature Range	25°C to +85°C
Storage Temperature Range	65°C to +150°C
Input Voltage	Equal to Supply Voltage
Logic to Logic Reference Differential Voltage[1]	+7V, -30V
Output Short Circuit Duration	Indefinite
Hold Capacitor Short Circuit Duration	10s
Lead Temperature (soldering, 10s)	300°C

NOTE: (1) Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BURN-IN SCREENING

Burn-in screening is available for both plastic and TO-99 metal can packages. Burn-in duration is 160 hours at the temperature (or equivalent combination of time and temperature) indicated below:

Plastic "-BI" models: +85°C
TO-99 "-BI" models: +125°C

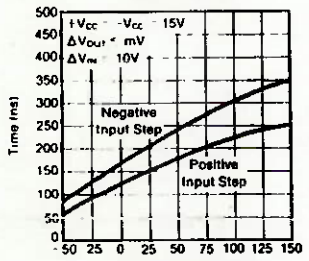
All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

ORDERING INFORMATION

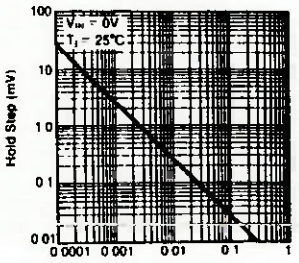
Model	Package	Temperature Range
SHC298AM	TO-99	25°C to +85°C
SHC298JP	8-pin DIP	0°C to +70°C
SHC298JU	8-lead SOIC	0°C to +70°C
SHC298AJP	8-pin DIP	0°C to +70°C
BURN-IN SCREENING OPTION See text for details		
Model	**Package**	**Temperature Range**
SHC298AM-BI	TO-99	-25°C to +85°C
SHC298JP-BI	8-pin DIP	0°C to +70°C
SHC298JU-BI	8-lead SOIC	0°C to +70°C
SHC298AJP-BI	8-pin DIP	0°C to +70°C

TYPICAL PERFORMANCE CURVES

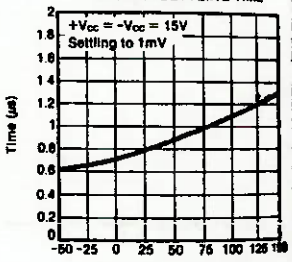
APERTURE TIME



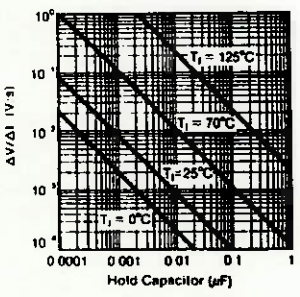
CHARGE OFFSET



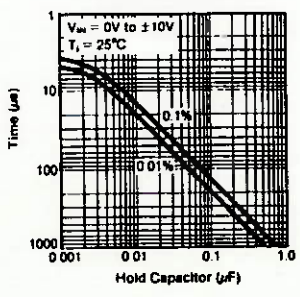
SAMPLE-TO-HOLD TRANSIENT SETTLING TIME



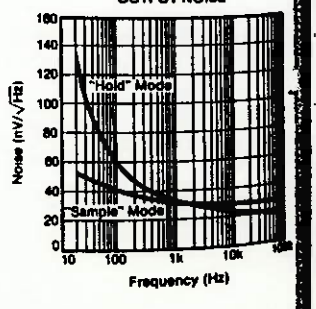
OUTPUT DROOP RATE



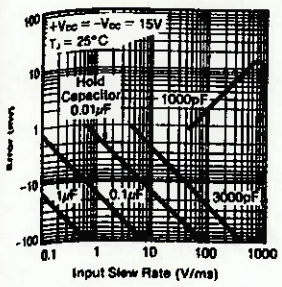
ACQUISITION TIME



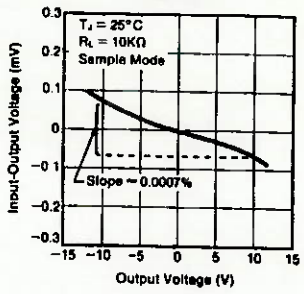
OUTPUT NOISE



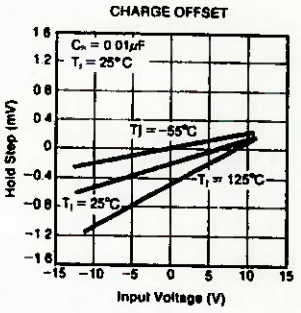
DYNAMIC SAMPLING ERROR



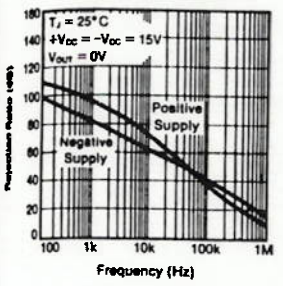
GAIN ERROR



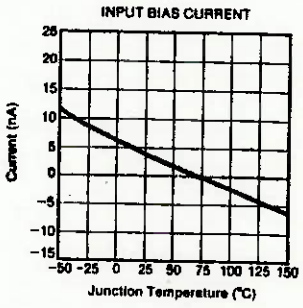
CHARGE OFFSET



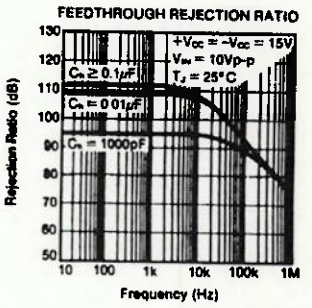
POWER SUPPLY REJECTION



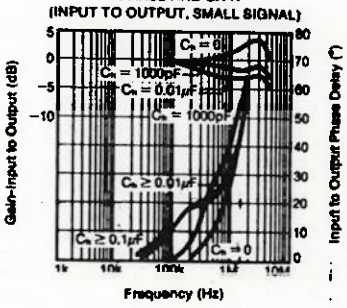
INPUT BIAS CURRENT



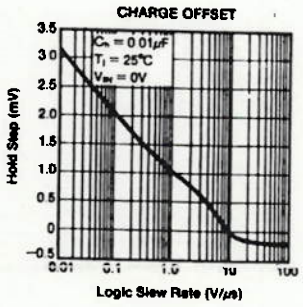
FEEDTHROUGH REJECTION RATIO



PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)



CHARGE OFFSET



DISCUSSION OF SPECIFICATIONS

THROUGHPUT NONLINEARITY

Throughput nonlinearity is defined as total Hold mode, nonadjustable, input to output error caused by charge offset, gain nonlinearity, 1ms of droop, feedthrough, and thermal transients. It is the inaccuracy due to these errors which cannot be corrected by offset and gain adjustments. Throughput nonlinearity is tested with a 1000pF holding capacitor, 10V input changes, 10µs acquisition time, and 1ms Hold time (see Figure 1).

GAIN ACCURACY

Gain Accuracy is the difference between Input and Output voltage (when in the Sample mode) due to amplifier gain errors.

DROOP RATE

Droop Rate is the voltage decay at the output when in the Hold mode due to storage capacitor, FET switch leakage currents, and output amplifier bias current.

FEEDTHROUGH

Feedthrough is the amount of the input voltage change that appears at the output when the amplifier is in the Hold mode.

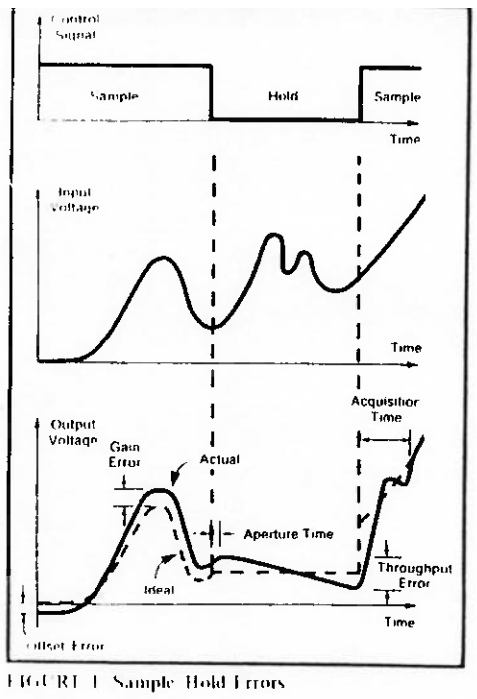


FIGURE 1. Sample Hold Errors.

APERTURE TIME

Aperture Time is the time required to switch from Sample to Hold. The time is measured from the 50% point of the mode control transition to the time at which the output stops tracking the input.

ACQUISITION TIME

Acquisition Time is the time required for the sample hold output to settle within a given error band of its final value when the mode control is switched from Hold to Sample.

CHARGE OFFSET

Charge Offset is the offset that results from the charge coupled through the gate capacitance of the switching FET. This charge is coupled into the storage capacitor when the FET is switched to the "hold" mode.

OPERATING INSTRUCTIONS

EXTERNAL CAPACITOR SELECTION

Capacitors with high insulation resistance and low dielectric absorption, such as teflon, polystyrene or polypropylene units, should be used as storage elements (polystyrene should not be used above +85°C). Care should be taken in the printed circuit layout to minimize AC and DC leakage currents from the capacitor to reduce chage offset and droop errors.

The value of the external capacitor determines the droop, charge offset and acquisition time of the Sample. Hold. Both droop and charge offset will vary linearly with capacitance from the values given in the specification table for a 0.001µF capacitor. With a capacitor of 0.01µF the droop will reduce to approximately 2.5µV/ms and the charge offset to approximately 1.5mV. The behavior of acquisition time with changes in external capacitance is shown in the Typical Performance Curves.

OFFSET ADJUSTMENT

The offset should be adjusted with the input grounded. During the adjustment, the sample/hold should be switching continuously between the Sample and the Hold mode. The error should then be adjusted to zero when the unit is in the Hold mode. In this way, charge offset as well as amplifier offset will be adjusted. When a 0.001µF capacitor is used, it will not be possible to adjust the full offset error at the sample/hold. It should be adjusted elsewhere in the system.

APPLICATIONS

DATA ACQUISITION

The SHC298 may be used to hold data for conversion with an analog-to-digital converter or used to provide Pulse Amplitude Modulation (PAM) data output (see Figures 2 and 3).

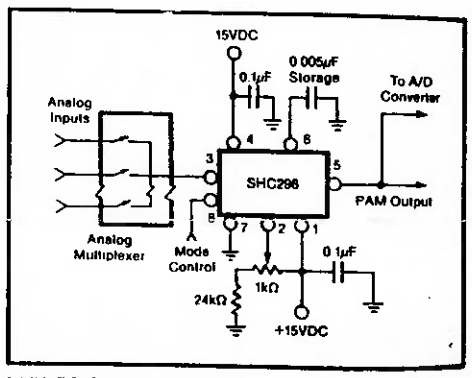


FIGURE 2. Data Acquisition.

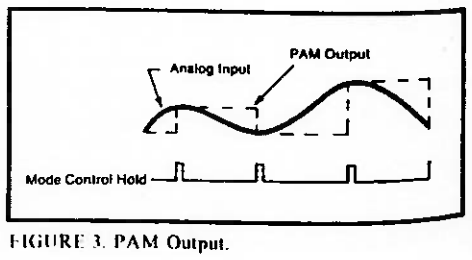


FIGURE 3. PAM Output.

DATA DISTRIBUTION

The SHC298 may be used to hold the output of a digital-to-analog converter whose digital inputs are multiplexed (see Figure 4).

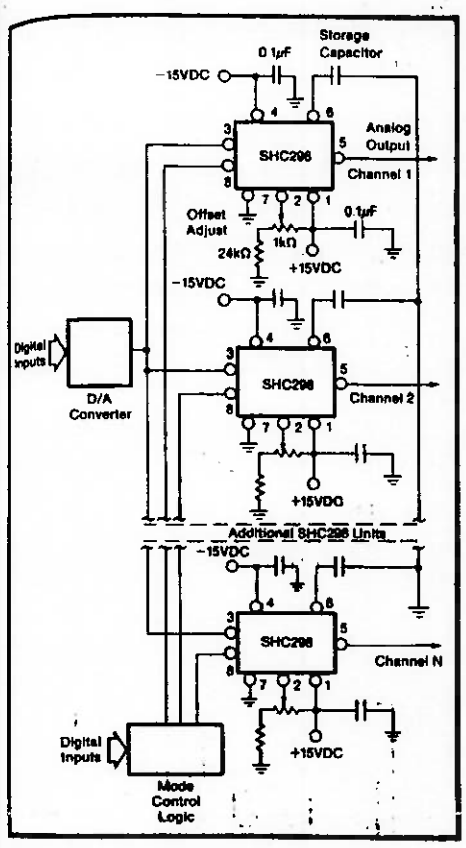


FIGURE 4. Data Distribution.

TEST SYSTEMS

The SHC298 is also well suited for use in test systems to acquire and hold data transients for human operators or for other parts of the test system such as comparators, digital voltmeters, etc.

With a 0.1µF storage capacitor, the output may be held 10 seconds with less than 0.1% error. With a 1µF storage capacitor, the output may be held more than 15 minutes with less than 1% error.

CAPACITIVE LOADING

SHC298 is sensitive to capacitive loading on the output and may oscillate. When driving long lines, a buffer should be used.

HIGH SPEED DATA ACQUISITION

The minimum sample time for one channel in a data acquisition system is usually considered to be the acquisition time of the sample/hold plus the conversion time of the analog-to-digital converter. If two or more sample/holds are used with a high-speed multiplexer, the acquisition time of the sample/hold can be virtually eliminated. While the first channel is in hold and switched on to the ADC, the multiplexer may be addressed to the next channel. The second sample/hold will have acquired this data by the time the conversion is complete. Then, the sample/holds reverse roles and another channel is addressed (see Figure 5). Fow low-level systems, and instrumentation amplifier and double-ended multiplexer may be connected to the sample/hold inputs. The settling time of the multiplexer, instrumentation amplifier, and sample/hold can be eliminated from the channel conversion time as before.

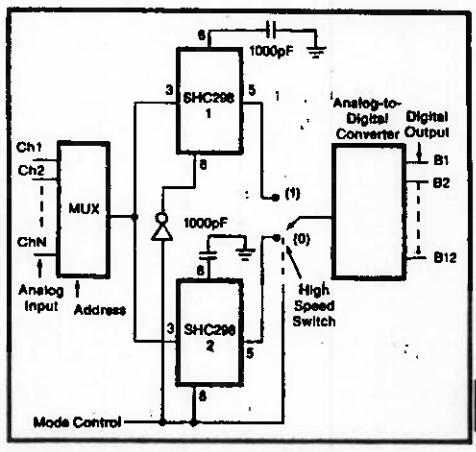


FIGURE 5. "Ping-Pong" Sample Holds.

MOTOROLA

MC14051B
MC14052B
MC14053B

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

ANALOG MULTIPLEXERS/ DEMULTIPLEXERS

ANALOG MULTIPLEXERS/DEMULTIPLEXERS

The MC14051B, MC14052B, and MC14053B analog multiplexers are digitally controlled analog switches. The MC14051B effectively implements an SPST solid state switch, the MC14052B a DP4T, and the MC14053B a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD} – V_{EE}) = 3 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Linearized Transfer Characteristics
- Low-Noise = 12 nV $\sqrt{Cycle}$, f = 1 kHz typical
- Pin-for-Pin Replacement for CD4051, CD4052, and CD4053
- For 4PDT Switch, See MC14551B
- For Lower R_{ON}, Use the HC4051, HC4052, or HC4053 High-Speed CMOS Devices

CASE 620
L SUFFIX
CERAMIC PACKAGE

CASE 648
P SUFFIX
PLASTIC PACKAGE

ORDERING INFORMATION

A Series = −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

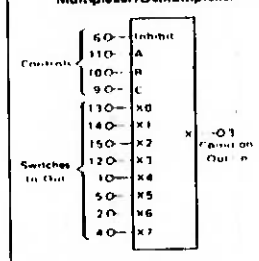
C Series = −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS*

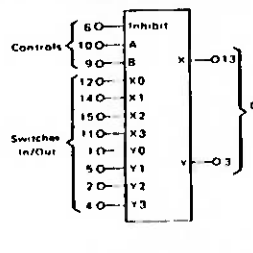
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage (Referenced to V_{EE} $V_{SS} \geq V_{EE}$)	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	−0.5 to V_{DD} +0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	±10	mA
I_{sw}	Switch Through Current	±25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

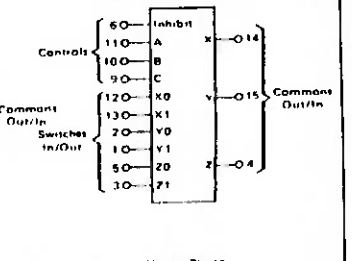
MC14051B
8-Channel Analog Multiplexer/Demultiplexer



MC14052B
Dual 4-Channel Analog Multiplexer/Demultiplexer



MC14053B
Triple 2-Channel Analog Multiplexer/Demultiplexer



Note: Control Inputs referenced to V_{SS}. Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

6

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ#	25°C Max	T_{high}* Min	T_{high}* Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}		V_{DD} = V_{SS} - V_{EE}	3	18	3		18	3	18	V
Quiescent Current Per Package (Figure 4)	I_{DD}	5 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD} Switch I/O: V_{in} = V_{EE} or V_{DD} and ΔV_{switch} = 500 mVdc		5 10 20		0.005 0.010 0.015	5 10 20		150 300 600	µA
Quiescent Current Per Package (Figure 4)	I_{DD}	5 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD} Switch I/O: V_{in} = V_{EE} or V_{DD} and ΔV_{switch} = 500 mVdc		20 40 80		0.005 0.010 0.015	20 40 80		150 300 600	µA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{T(AV)}$	5 10 15	T_A = 25°C only (All channels switching) (V_{in}, V_{out} @ f = fin, C_L not included)	Typical: (0.07 µA/kHz) f + I_{DD} (0.20 µA/kHz) f + I_{DD} (0.46 µA/kHz) f + I_{DD}							µA
CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5 10 15	R_{on} = per spec I_{off} = per spec		1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	V
High-Level Input Voltage	V_{IH}	5 10 15	R_{on} = per spec I_{off} = per spec	3.5 7.0 11.0		3.5 7.0 11.0	2.75 5.50 8.25		3.5 7.0 11.0		V
Input Leakage Current (All Inputs)	I_{in}	15	V_{in} = 0 or V_{DD}		±0.1		±0.00001	±0.1		±1.0	µA
Input Leakage Current (Inhibit Input)	I_{in}	15	V_{in} = 0 or V_{DD}		±0.3		±0.00001	±0.3		±1.0	µA
Input Capacitance	C_{in}						5.0	7.5			pF
SWITCHES IN/OUT AND COMMONS OUT/IN - X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{(IO)}$		Channel On or Off	0	V_{DD}	0		V_{DD}	0	V_{DD}	Vpp
Feedthrough Voltage Across Switch (Figure 5)	ΔV_{Switch}		Channel On	0	500	0		600	0	300	mV
Offset Voltage	V_{OO}		V_{in} = 0 V, No load				10				µV
On Resistance (Figure 6)	R_{on}	5 10 15	ΔV_{switch} = 500 mVdc V_{in} = V_{IL} or V_{IH} (Control) and V_{in} = 0 to V_{DD} (Switch)		800 400 320		250 120 80	1050 500 280		1300 550 120	Ω
On Resistance (Figure 6)	R_{on}	5 10 15	ΔV_{switch} = 500 mVdc V_{in} = V_{IL} or V_{IH} (Control) and V_{in} = 0 to V_{DD} (Switch)		800 400 320		250 120 80	1050 500 280		1200 520 300	Ω
Δ On Resistance Between Any Two Channels or Same Package	ΔR_{on}	5 10 15			70 50 45		25 10 10	70 50 45		135 95 85	Ω
Off Channel Leakage Current (All Types) (Figure 10)	I_{off}	15	V_{in} = V_{IL} or V_{IH} (Control) Channel to Channel or Any One Channel		±100		±0.05	±100		±1000	nA
Off Channel Leakage Current (Common Out/In) (Figure 10)	I_{off}	15	V_{in} = V_{IL} or V_{IH} (Control) Channel to Channel or Any One Channel		±100		±0.05	±400		±1000	nA
Switch Input Capacitance	C_{IS}		Input = V_{DD}				10				pF
Common Output/Input Capacitance	C_{OS}		Inhibit = V_{DD} (MC14051B) (MC14052B) (MC14053B)				60 32 17				pF
Feedthrough Capacitance (Figure 11)	C_{FD}		Pins Not Adjacent Pins Adjacent				0.15 0.47				pF

*T_{low} = -55°C for AF Device, -40°C for CL/CP Device
T_{high} = +125°C for AF Device, +85°C for CL/CP Device
#Data labelled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive $V_{O(I)}$ current may be drawn, i.e., the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C) (V_{EE} = V_{SS} unless otherwise indicated)

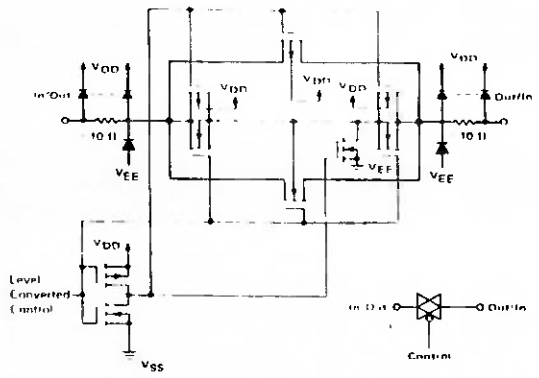
Characteristic	Symbol	V_{DD} V_{EE} Vdc	Typ # All Types	Max	Unit
Propagation Delay Times (Figure 8)	t_{PLH}, t_{PHL}				ns
Switch Input to Switch Output (R_L = 10 kΩ)					
MC14051					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	90	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	30	
MC14052					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	75	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	30	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	25	
MC14053					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	65	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	15	
Inhibit to Output (R_L = 10 kΩ, V_{EE} = V_{SS})					
Output "1" or "0" to High Impedance, or High Impedance to "1" or "0" Level	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}				ns
MC14051B		5.0	350	700	
		10	170	340	
		15	140	280	
MC14052B		5.0	300	600	ns
		10	150	310	
		15	125	250	
MC14053B		5.0	275	550	ns
		10	140	280	
		15	110	220	
Control Input to Output (R_L = 10 kΩ, V_{EE} = V_{SS})	t_{PLH}, t_{PHL}				ns
MC14051B		5.0	380	720	
		10	160	320	
		15	120	240	
MC14052B		5.0	325	650	ns
		10	130	260	
		15	90	180	
MC14053B		5.0	300	600	ns
		10	120	240	
		15	80	160	
Second Harmonic Distortion (R_L = 10KΩ, f = 1kHz) V_{in} = 5 Vpp	-	10	0.07	–	%
Bandwidth (Figure 7) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} - V_{EE}) p-p, C_L = 50pF 20 Log $\frac{V_{out}}{V_{in}}$ = -3 dB)	BW	10	17	—	MHz
Off Channel Feedthrough Attenuation (Figure 7) (R_L = 1KΩ, V_{in} = 1/2 (V_{DD} - V_{EE}) p-p f_{in} = 4.5 MHz — MC14051B f_{in} = 30 MHz — MC14052B f_{in} = 55 MHz — MC14053B	–	10	50	—	dB
Channel Separation (Figure 8) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD} - V_{EE}) p-p, f_{in} = 3.0 MHz	–	10	50	–	dB
Crosstalk, Control Input to Common O/I (Figure 9) (R_t = 1 kΩ, R_L = 10 kΩ Control t_{TLH} = t_{THL} = 20 ns, Inhibit = V_{SS})	–	10	75	–	mV

*The formulas given are for the typical characteristics only at 25°C
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE}, or V_{DD}). Unused outputs must be left open.

FIGURE 1 – SWITCH CIRCUIT SCHEMATIC



TRUTH TABLE

Control Inputs				ON Switches		
	Select					
Inhibit	C*	B	A	MC14051B	MC14052B	MC14053B
0	0	0	0	X0	Y0 X0	Z0 Y0 X0
0	0	0	1	X1	Y1 X1	Z0 Y0 X1
0	0	1	0	X2	Y2 X2	Z0 Y1 X0
0	0	1	1	X3	Y3 X3	Z0 Y1 X1
0	1	0	0	X4		Z1 Y0 X0
0	1	0	1	X5		Z1 Y0 X1
0	1	1	0	X6		Z1 Y1 X0
0	1	1	1	X7		Z1 Y1 X1
1	x	x	x	None	None	None

*Not applicable for MC14052
x = Don't Care

FIGURE 2 – MC14051B FUNCTIONAL DIAGRAM

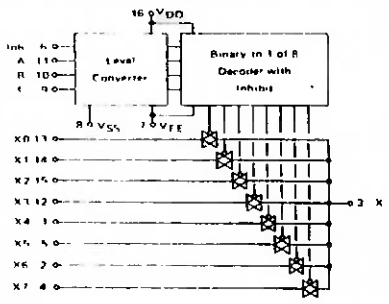


FIGURE 3 – MC14052B FUNCTIONAL DIAGRAM

FIGURE 4 – MC14053B FUNCTIONAL DIAGRAM

TEST CIRCUITS

FIGURE 5 – ΔV ACROSS SWITCH

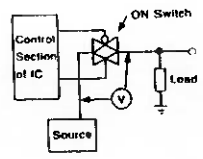


FIGURE 6 – PROPAGATION DELAY TIMES, CONTROL AND INHIBIT TO OUTPUT

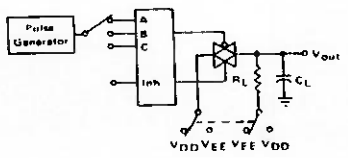


FIGURE 7 – BANDWIDTH AND OFF-CHANNEL FEEDTHROUGH ATTENUATION

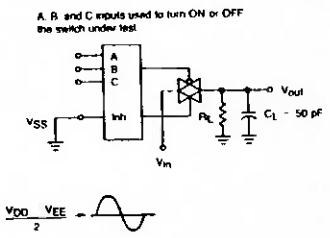


FIGURE 8 – CHANNEL SEPARATION (ADJACENT CHANNELS USED FOR SETUP)

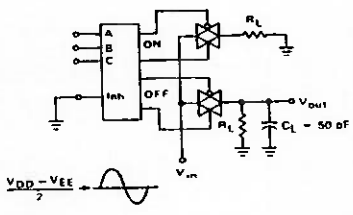
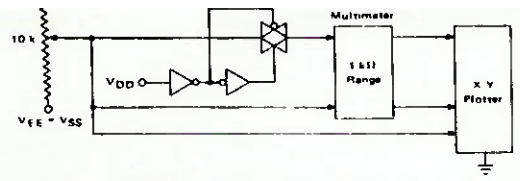


FIGURE 9 – CROSSTALK, CONTROL INPUT TO COMMON O/I

FIGURE 10 – OFF CHANNEL LEAKAGE



TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 12 – V_{DD} = 7.5 V, V_{EE} = -7.5 V

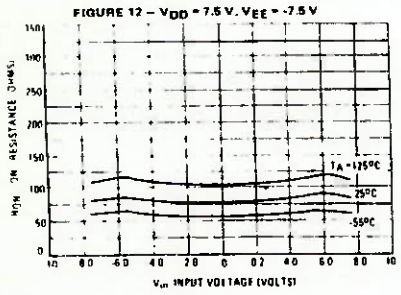


FIGURE 13 – V_{DD} = 5.0 V, V_{EE} = -5.0 V

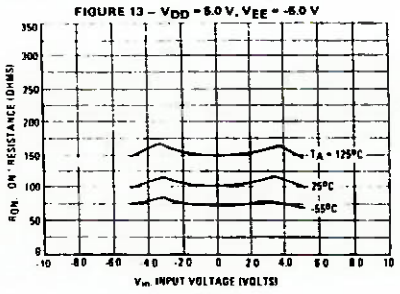


FIGURE 14 – V_{DD} = 2.5 V, V_{EE} = -2.5 V

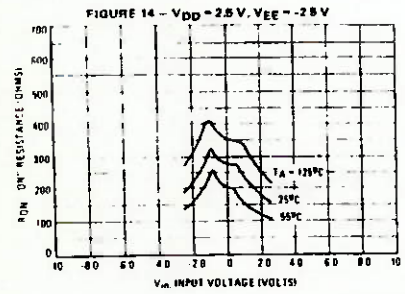
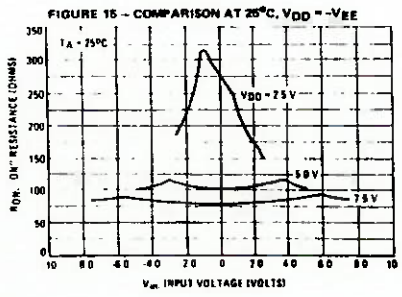
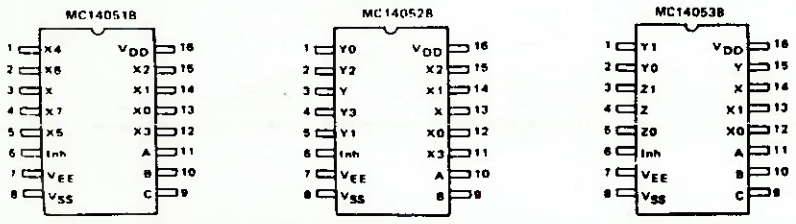


FIGURE 15 – COMPARISON AT 25°C, V_{DD} = -V_{EE}



PIN ASSIGNMENT



V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = +5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} – V_{SS} = 5 V maximum swing above V_{SS}; V_{SS} – V_{EE} = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V

the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = +10 V, V_{SS} = +5 V, and V_{EE} = −3 V is acceptable. See the Table below.

FIGURE A — APPLICATION EXAMPLE

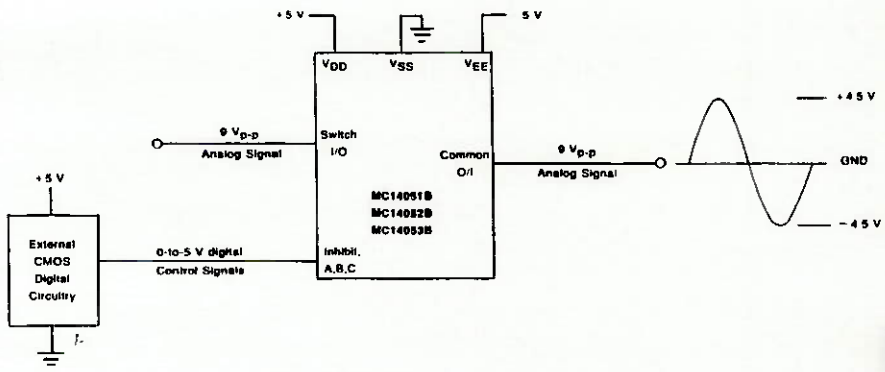
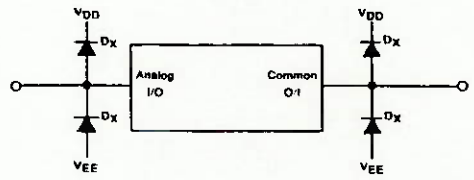


FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES



POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+8	0	-8	+8/0	+8 to -8 = 16 V_{p-p}
+5	0	-12	+5/0	+5 to -12 = 17 V_{p-p}
+5	0	0	+5/0	+5 to 0 = 5 V_{p-p}
+5	0	-5	+5/0	+5 to -5 = 10 V_{p-p}
+10	+5	-5	+10/+5	+10 to -5 = 15 V_{p-p}

TYPES SN54LS373, SN54LS374, SN54S373, SN54S374
SN74LS373, SN74LS374, SN74S373, SN74S374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

OCTOBER 1975—REVISED

- Choice of 8 Latches or 8 D-Type Flip-Flops In a Single Package
- 3-State Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection ('S373 and 'S374)
- P-N-P Inputs Reduce D-C Loading on Data Lines ('S373 and 'S374)

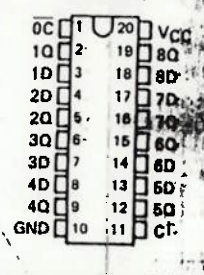
'LS373, 'S373
FUNCTION TABLE

OUTPUT ENABLE	ENABLE LATCH	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

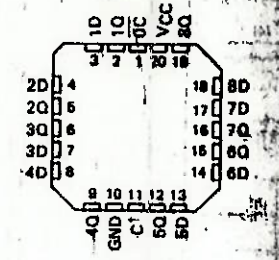
'LS374, 'S374
FUNCTION TABLE

OUTPUT ENABLE	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN54LS373, SN54LS374, SN54S373, SN54S374 . . . J PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS373, SN54LS374, SN54S373, SN54S374 . . . FK PACKAGE
SN74LS373, SN74LS374, SN74S373, SN74S374 . . . FN PACKAGE
(TOP VIEW)



IC for 'LS373 and 'S373, CLK for 'LS374 and 'S374

description

These 8-bit registers feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (C) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

PRODUCTION DATA
This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

description (continued)

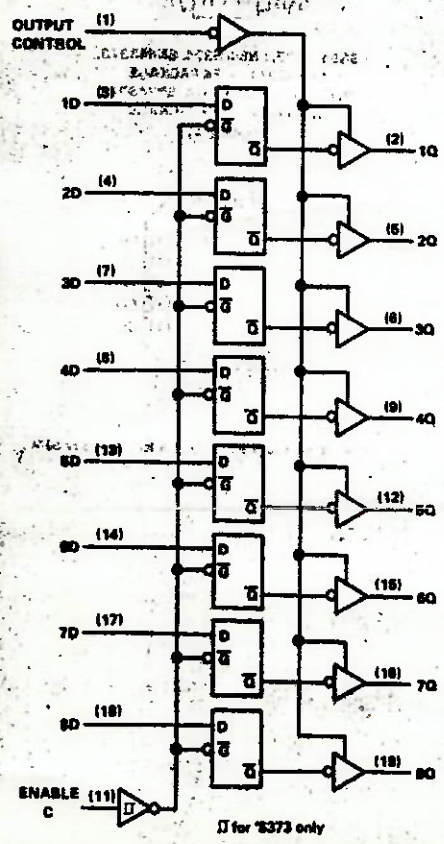
The eight flip-flops of the 'LS374 and 'S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines of the 'S373 and 'S374 devices, simplify system design as ac and noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

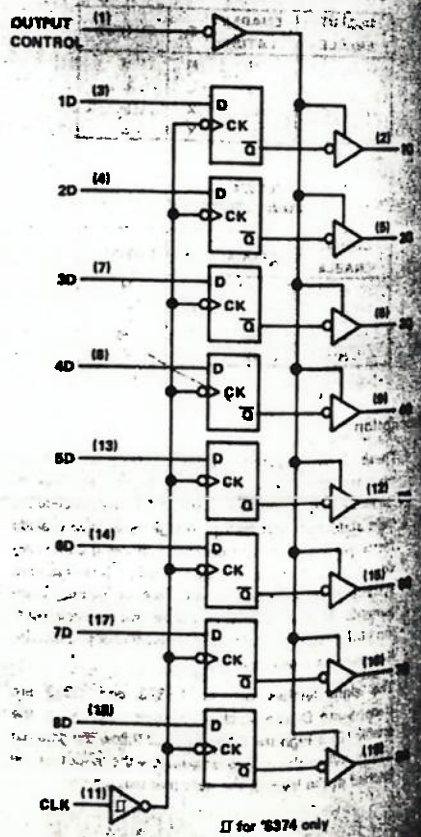
logic diagrams

'LS373, 'S373
TRANSPARENT LATCHES



Π for 'S373 only

'LS374, 'S374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS



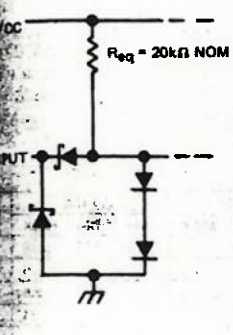
Π for 'S374 only

Pin numbers shown on logic notation are for DW, J or N packages.

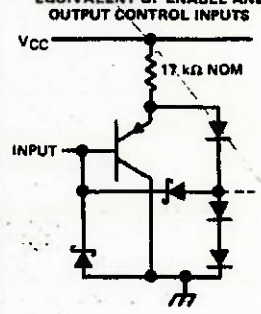
...tic of inputs and outputs

'LS373

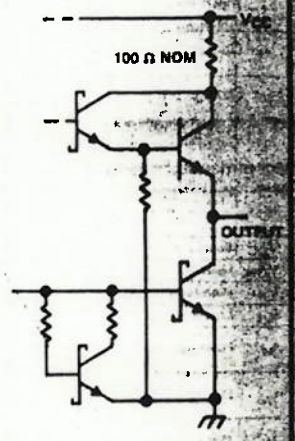
EQUIVALENT OF DATA INPUTS



EQUIVALENT OF ENABLE AND OUTPUT CONTROL INPUTS

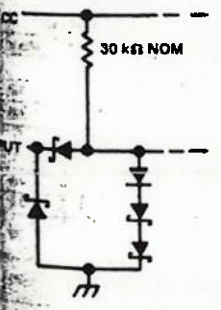


TYPICAL OF ALL OUTPUTS

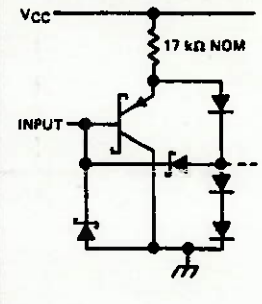


'LS374

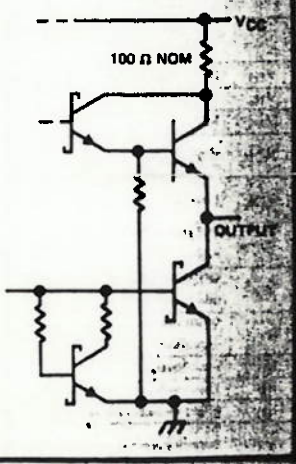
EQUIVALENT OF DATA INPUTS



EQUIVALENT OF CLOCK AND OUTPUT CONTROL INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High-level output voltage				5.5			5.5	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	CLK high	15			15			ns
		CLK low	15			15			
t_{su}	Data setup time	'LS373	5↓			5↓			ns
		'LS374	20↑			20↑			
t_h	Data hold time	'LS373	20↓			20↓			ns
		'LS374†	0↑			0↑			
T_A	Operating free-air temperature		−55		125	0		70	°C

† The t_h specification applies only for data frequency below 10 MHz. Designs above 10 MHz should use a minimum of 5 ns.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, Output control at 4.5 V	'LS373		24	40		24	40	mA
			'LS374		27	40		27	40	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

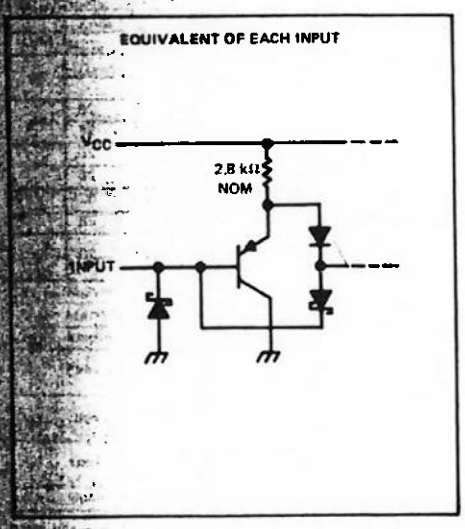
switching characteristics, V_{CC} = 5 V, T_A = 25°C

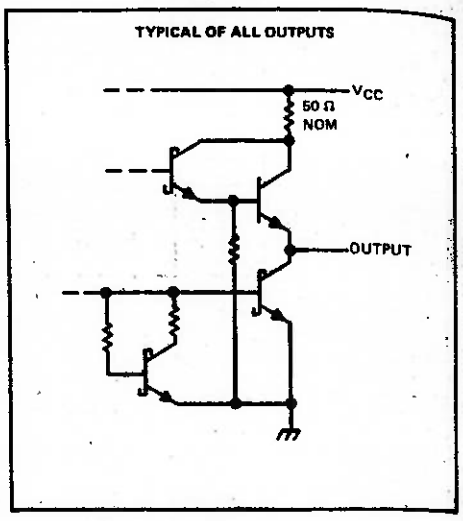
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS373 MIN	'LS373 TYP	'LS373 MAX	'LS374 MIN	'LS374 TYP	'LS374 MAX	UNIT
f_{max}			C_L = 45 pF, R_L = 667 Ω, See Notes 2 and 3					35	50		MHz
t_{PLH}	Data	Any Q				12	18				ns
t_{PHL}						12	18				
t_{PLH}	Clock or strobe	Any Q				20	30		15	28	ns
t_{PHL}						18	30		19	28	
t_{PZH}	Output Control	Any Q				15	28		20	26	ns
t_{PZL}						25	36		21	28	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 667 Ω, See Note 3	SN54		28	32		28	32	ns
				SN74		15	25		15	28	
t_{PLZ}	Output Control	Any Q				12	20		12	20	ns

NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
3. See General Information Section for load circuits and voltage waveforms.

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

schematic of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' . . . . . −55°C to 125°C
SN74S' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S'			SN74S'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
High-level output current, I_{OH}				−2			−6.5	mA
Width of clock/enable pulse, t_w	High	6			6			ns
	Low	7.3			7.3			
Data setup time, t_{su}	'S373	0↓			0↓			ns
	'S374	5↑			5↑			
Data hold time, t_h	'S373	10↓			10↓			ns
	'S374	2↑			2↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†				MIN	TYP‡	MAX	UNIT
V_{IH}						2			V
V_{IL}								0.8	V
V_{IK}		V_{CC} = MIN,	I_I = −18 mA					−1.2	V
V_{OH}	SN54S'	V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OH} = MAX	2.4	3.4		V
	SN74S'					2.4	3.1		
V_{OL}		V_{CC} = MIN,	V_{IH} = 2 V,	V_{IL} = 0.8 V,	I_{OL} = 20 mA			0.5	V
I_{OZH}		V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.4 V				50	μA
I_{OZL}		V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 0.5 V				−50	μA
I_I		V_{CC} = MAX,	V_I = 5.5 V					1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V					50	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.5 V					−250	μA
I_{OS}§		V_{CC} = MAX				−40		−100	mA
I_{CC}		V_{CC} = MAX	'S373		outputs high			160	mA
					outputs low			160	
					outputs disabled			190	
			'S374		outputs high			110	
					outputs low			140	
					outputs disabled			160	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

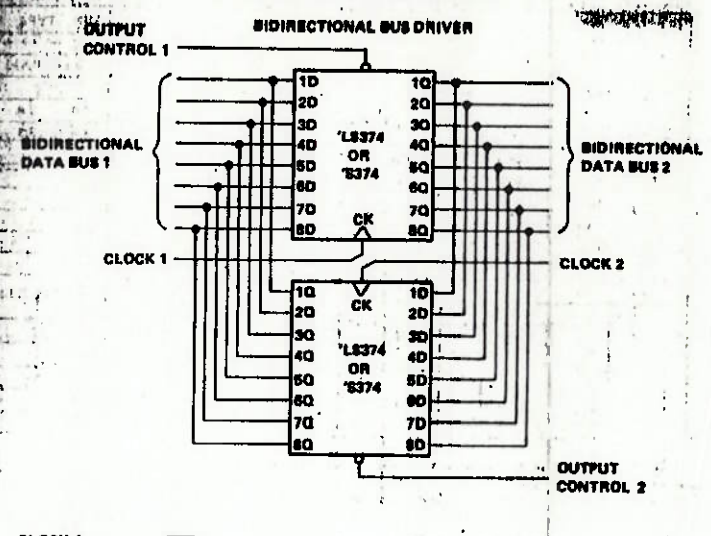
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S373			'S374			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}							75	100		MHz
t_{PLH}	Data	Any Q	C_L = 15 pF, R_L = 280 Ω, See Notes 2 and 4		7	12				ns
t_{PHL}					7	12				
t_{PLH}	Clock or enable	Any Q			7	14		8	15	ns
t_{PHL}					12	18		11	17	
t_{PZH}	Output Control	Any Q			8	15		8	15	ns
t_{PZL}					11	18		11	18	
t_{PHZ}	Output Control	Any Q	C_L = 5 pF, R_L = 280 Ω, See Note 3		8	9		8	9	ns
t_{PLZ}					8	12		7	12	

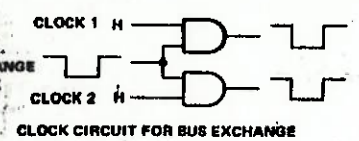
NOTES: 2. Maximum clock frequency is tested with all outputs loaded.
4. See General Information Section for load circuits and voltage waveforms.

f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
t_{PZH} = output enable time to high level
t_{PZL} = output enable time to low level
t_{PHZ} = output disable time from high level
t_{PLZ} = output disable time from low level

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

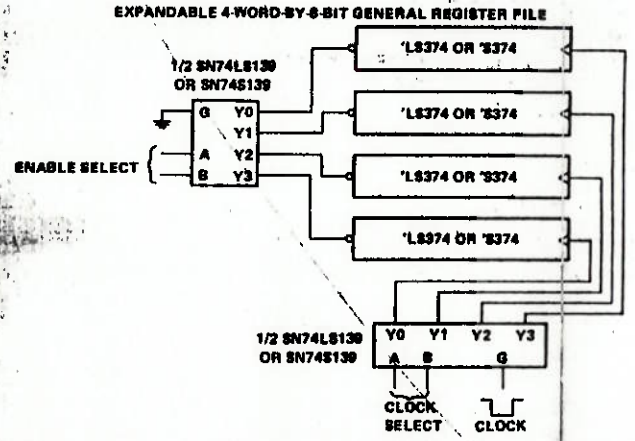
TYPICAL APPLICATION DATA





CLOCK CIRCUIT FOR BUS EXCHANGE

EXPANDABLE 4-WORD-BY-8-BIT GENERAL REGISTER FILE



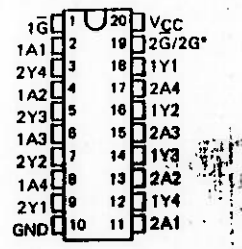
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN54LS240, SN54LS241, SN54LS244, SN54S240, SN54S241, SN54S...
SN74LS240, SN74LS241, SN74LS244, SN74S240, SN74S241, SN74S...
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

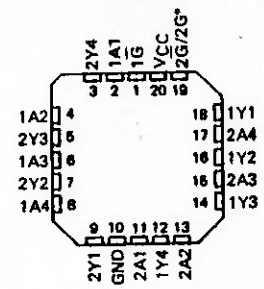
REVISED APRIL 1985

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce D-C Loading
- Hysteresis at Inputs Improves Noise Margins

SN54LS', SN54S' . . . J PACKAGE
SN74LS', SN74S' . . . DW, J OR N PACKAGE
(TOP VIEW)



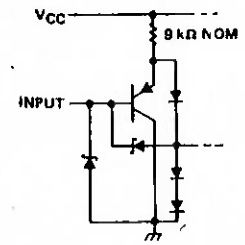
SN54LS', SN54S' . . . FK PACKAGE
SN74LS', SN74S' . . . FN PACKAGE
(TOP VIEW)



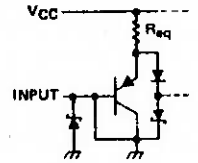
*2G for 'LS241 and 'S241 or 2$\overline{G}$ for all other drivers.

schematics of inputs and outputs

'LS240, 'LS241, 'LS244
EQUIVALENT OF EACH INPUT

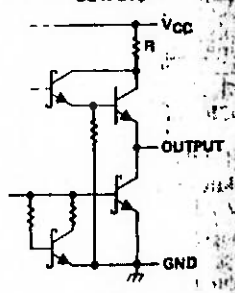


'S240, 'S241, 'S244
EQUIVALENT OF EACH INPUT



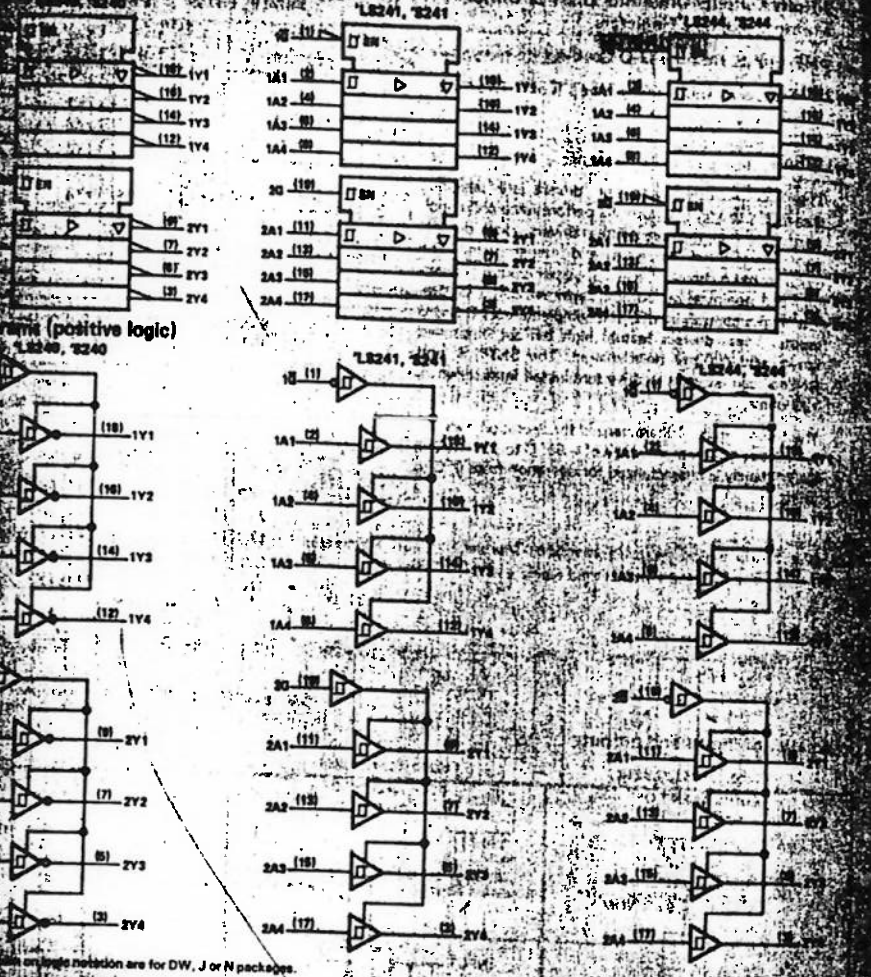
G and $\overline{G}$ inputs: R_{eq} = 2 kΩ NOM
A inputs: R_{eq} = 2.8 kΩ NOM

TYPICAL OF ALL OUTPUTS



'LS240, 'LS241, 'LS244:
R = 50 Ω NOM
'S240, 'S241, 'S244
R = 25 Ω NOM

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265



(positive logic)

...notation are for DW, J or N packages.

...ratings over operating free-air temperature range (unless otherwise noted)

...V_{CC} (see Note 1) . . . . . 7 V
...voltage: 'LS Circuits . . . . . 7 V
'S Circuits . . . . . 5.5 V
...state output voltage . . . . . 5.5 V
...rating free-air temperature range: SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
...age temperature range . . . . . −65°C to 150°C

...voltage values are with respect to network ground terminal.

...operating conditions

...Parameter	SN54LS' MIN	NOM	MAX	SN74LS' MIN	NOM	MAX	UNIT
...Supply voltage (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
...High-level input voltage	2			2			V
...Low-level input voltage			0.7			0.8	V
...High-level output current			−12			−15	mA
...Low-level output current			12			24	mA
...Operating free-air temperature	−55		125	0		70	°C

...voltage values are with respect to network ground terminal.

...characteristics over recommended operating free-air temperature range (unless otherwise noted)

...Parameter	...Test conditions		SN54LS' MIN	TYP‡	MAX	SN74LS' MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
...hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN		0.2			0.2			V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −3 mA		2.4	3.4		2.4	3.4		V
	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX		2			2			V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 4 mA			0.4			0.4	V
		I_{OL} = 8 mA						0.5	
I_{OZH}	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.7 V			20			20	μA
I_{OZL}		V_O = 0.4 V			−20			−20	μA
I_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_{OS}	Outputs high		−40		−225	−40		−225	mA
I_{CC}	Outputs low	All		17	27		17	27	mA
	Outputs disabled	'LS240		26	44		26	44	
		'LS241, 'LS244		27	46		27	46	
	All outputs disabled	'LS240		29	50		29	50	
		'LS241, 'LS244		32	54		32	54	

...characteristics at MIN or MAX operating conditions, are tested under recommended operating conditions.
...input values except V_{CC} = 4.5 V or 5 V.
...not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

...switching characteristics, V_{CC} = 5 V, T_A = 25°C

...Parameter	...Test conditions		'LS240 MIN	TYP	MAX	'LS241, 'LS244 MIN	TYP	MAX	UNIT
...PLH	R_L = 667 Ω, See Note 2	C_L = 45 pF,		9	14		12	18	ns
...PHL				12	18		12	18	ns
...PZH				20	30		20	30	ns
...PZH				15	23		15	23	ns
...PLZ	R_L = 667 Ω, See Note 2	C_L = 5 pF,		10	20		10	20	ns
...PHZ				15	25		15	25	ns

...See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

PARAMETER	SN54S' MIN	SN54S' NOM	SN54S' MAX	SN74S' MIN	SN74S' NOM	SN74S' MAX	UNIT
Supply voltage, (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage	2			2			V
Low-level input voltage			0.8			0.8	V
High-level output current			−12			−15	mA
Low-level output current			48			64	mA
External resistance between any input and V_{CC} or ground			40			40	kΩ
Operating free-air temperature (see Note 3)	−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
3. An SN54S241J operating at free-air temperature above 116°C requires a heat sink that provides a thermal resistance from case to free-air $R_{\theta CA}$, of not more than 40°C/W.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

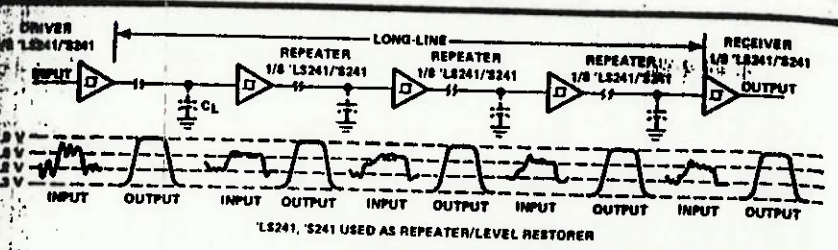
PARAMETER	TEST CONDITIONS†			SN54S' MIN	SN54S' TYP‡	SN54S' MAX	SN74S' MIN	SN74S' TYP‡	SN74S' MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = −18 mA					−1.2			−1.2	V
V_{hys} (V_{T+} − V_{T-})	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	V_{CC} = MIN, I_{OH} = −1 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,				2.7			V
	V_{CC} = MIN, I_{OH} = −3 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.4		2.4	3.4		V
	V_{CC} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.5 V,	2			2			V
V_{OL}	V_{CC} = MIN, I_{OL} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.55			0.55	V
I_{OZH}	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{IL} = 0.8 V,		V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V				50			50	μA
I_{IL} Any A	V_{CC} = MAX,	V_I = 0.5 V				−400			−400	μA
I_{IL} Any G						−2			−2	mA
I_{OS}	V_{CC} = MAX			−50		−225	−50		−225	mA
I_{CC} Outputs high	V_{CC} = MAX,	Outputs open	'240		80	123		80	135	mA
			'241, '244		95	147		95	160	
I_{CC} Outputs low			'240		100	148		100	160	
			'241, '244		120	170		120	180	
I_{CC} Outputs disabled			'240		100	145		100	150	
			'241, '244		120	170		120	180	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

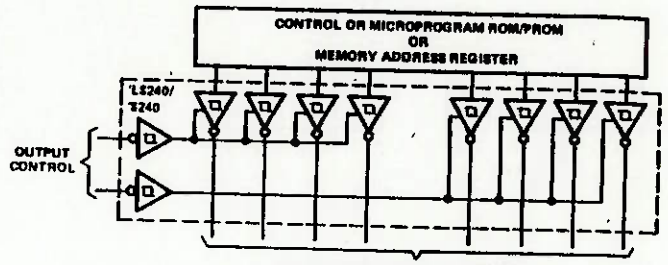
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	'240 MIN	'240 TYP	'240 MAX	'241, '244 MIN	'241, '244 TYP	'241, '244 MAX	UNIT
t_{PLH}	R_L = 90 Ω, C_L = 50 pF, See Note 4		4.5	7		6	9	ns
t_{PHL}			4.5	7		6	9	ns
t_{PZL}			10	18		10	18	ns
t_{PZH}			6.5	10		6	12	ns
t_{PLZ}	R_L = 90 Ω, C_L = 5 pF, See Note 4		10	15		10	15	ns
t_{PHZ}			6	9		6	9	ns

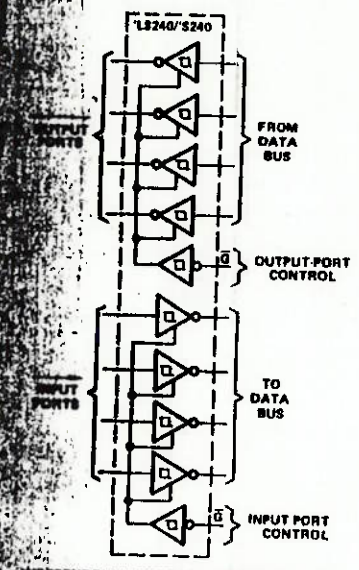
NOTE 4: See General Information Section for load circuits and voltage waveforms.



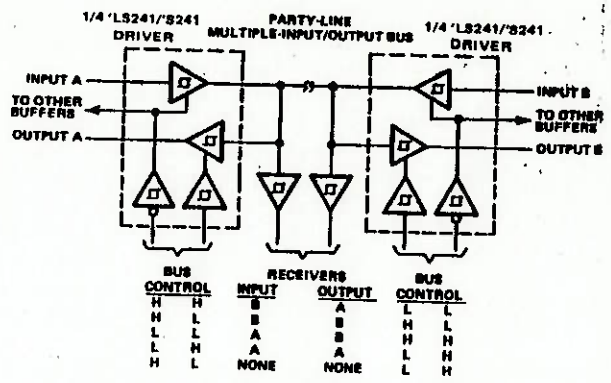
'LS241, 'S241 USED AS REPEATER/LEVEL RESTORER



'LS240/'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



BUS CONTROL		RECEIVERS INPUT	RECEIVERS OUTPUT	BUS CONTROL	
H	H	B	A	L	L
H	L	B	B	L	H
L	H	A	A	H	L
L	L	A	B	H	H
		NONE	NONE		

PARTY-LINE BUS SYSTEM
WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN5402, SN54L02, SN54LS02, SN54S02, SN7402, SN74LS02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

REVISED DECEMBER 1981

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain four independent 2-input NOR gates.

The SN5402, SN54L02, SN54LS02 and SN54S02 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7402, SN74LS02 and SN74S02 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

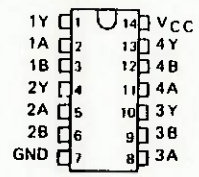
INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

logic diagram (each gate)

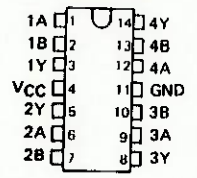
positive logic

$Y = \overline{A} \cdot \overline{B}$ or $Y = \overline{A + B}$

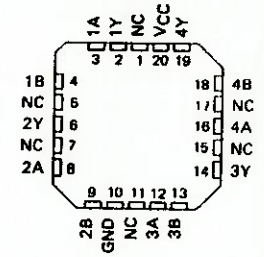
SN5402, SN54L02 . . . J PACKAGE
SN54LS02, SN54S02 . . . J OR W PACKAGE
SN7402 . . . J OR N PACKAGE
SN74LS02, SN74S02 . . . D, J OR N PACKAGE
(TOP VIEW)



SN5402 . . . W PACKAGE
(TOP VIEW)



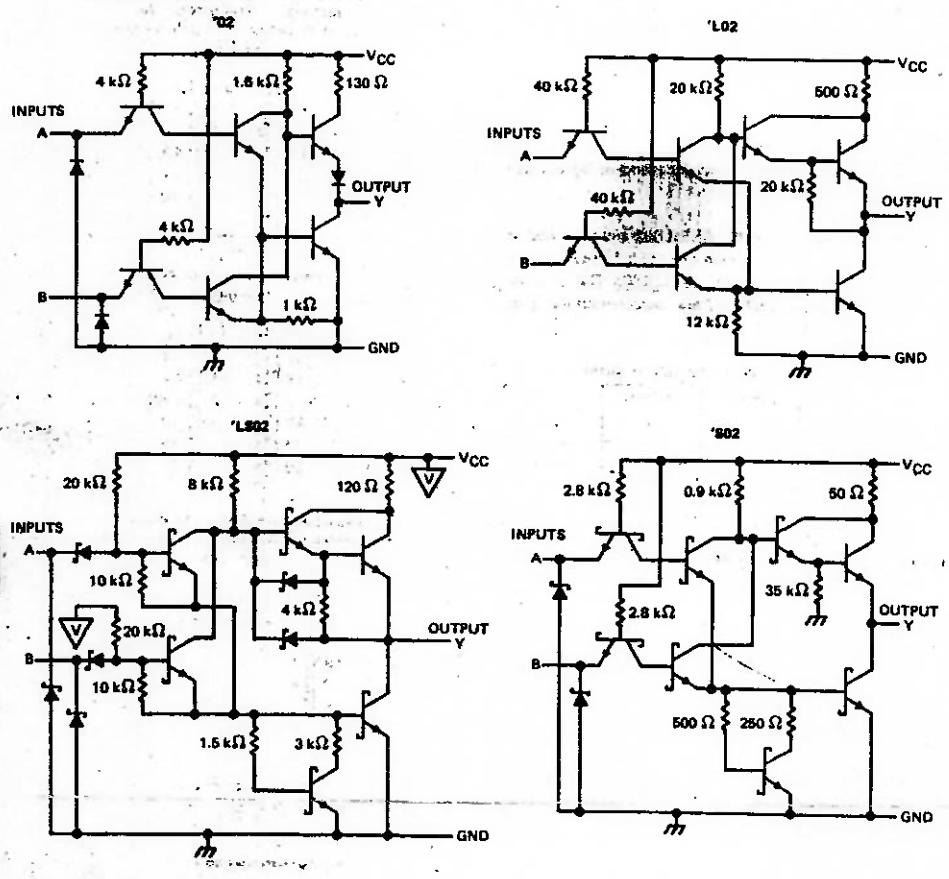
SN54LS02, SN54S02 . . . FK PACKAGE
SN74LS02, SN74S02 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

schematics (each gate)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '02, 'LS02, 'S02 ..... 7 V
'L02 ..... 8 V
Input voltage: '02, 'L02, 'S02 ..... 5.5 V
'LS02 ..... 7 V
Off-state output voltage ..... 7 V
Operating free-air temperature range: SN54' ..... −55°C to 125°C
SN74' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5402			SN7402			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			16			16	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5402			SN7402			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −0.4 mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		8	16		8	16	mA
I_{CCL}	V_{CC} = MAX, See Note 2		14	27		14	27	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 400 Ω, C_L = 15 pF		12	22	ns
t_{PHL}					8	15	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms

recommended operating conditions

	SN54L02			UNIT
	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.7	V
I_{OH} High-level output current			−0.1	mA
I_{OL} Low-level output current			2	mA
T_A Operating free-air temperature	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54L02			UNIT
		MIN	TYP‡	MAX	
V_{OH}	V_{CC} = MIN, V_{IL} = 0.7 V, I_{OH} = −0.1 mA	2.4	3.3		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 2 mA		0.15	0.3	V
I_I	V_{CC} = MAX, V_I = 5.5 V			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V			10	μA
I_{IL}	V_{CC} = MAX, V_I = 0.3 V			−0.18	mA
I_{OS}§	V_{CC} = MAX	−3		−15	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		0.8	1.6	mA
I_{CCL}	V_{CC} = MAX, See Note 2		1.4	2.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 4 kΩ, C_L = 50 pF		31	60	ns
t_{PHL}					35	60	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions

	SN54LS02			SN74LS02			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.7			0.8	V
I_{OH} High-level output current			−0.4			−0.4	mA
I_{OL} Low-level output current			4			8	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS02			SN74LS02			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −0.4 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}§	V_{CC} = MAX	−20		−100	−20		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		1.6	3.2		1.6	3.2	mA
I_{CCL}	V_{CC} = MAX, See Note 2		2.8	5.4		2.8	5.4	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 2 kΩ, C_L = 15 pF		10	15	ns
t_{PHL}					10	15	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms

TYPES SN54S02, SN74S02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

recommended operating conditions

		SN54S02			SN74S02			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S02			SN74S02			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
I_{IL}	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		17	29		17	29	mA
I_{CCL}	V_{CC} = MAX, See Note 2		28	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	R_L = 280 Ω, C_L = 15 pF		3.5	5.5	ns
t_{PHL}					3.5	5.5	ns
t_{PLH}			R_L = 280 Ω, C_L = 50 pF		5		ns
t_{PHL}					5		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

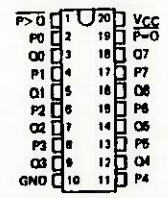
8-BIT MAGNITUDE/IDENTITY COMPARATORS

D2617, JANUARY 1981 – REVISED DECEMBER 1983

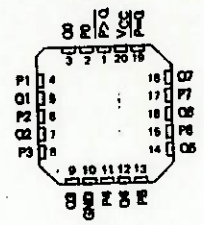
- Compares Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 and 'LS683 have 20-kΩ Pullup Resistors on the Q Inputs
- 'LS686 and 'LS687 . . . New JT and NT 24-Pin, 3000-Mil Packages

TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-kΩ PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS683	yes	yes	no	open-collector	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
'LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open-collector	no
'LS688	yes	no	yes	totem-pole	no
'LS689	yes	no	yes	open-collector	no

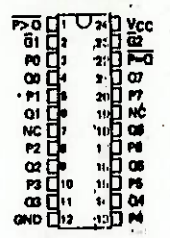
SN54LS682 THRU SN54LS685 . . . J PACKAGE
SN74LS682 THRU SN74LS685 . . . DW, J OR N PACKAGE
(TOP VIEW)



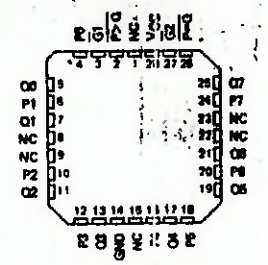
SN54LS682 THRU SN54LS685 . . . FK PACKAGE
SN74LS682 THRU SN74LS685 . . . FN PACKAGE
(TOP VIEW)



SN54LS686, SN54LS687 . . . JT PACKAGE
SN74LS686, SN74LS687 . . . DW, JT OR NT PACKAGE
(TOP VIEW)

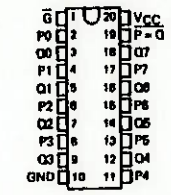


SN54LS686, SN54LS687 . . . FK PACKAGE
SN74LS686, SN74LS687 . . . FN PACKAGE
(TOP VIEW)

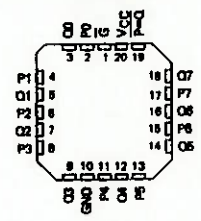


NC – No internal connection

SN54LS688, SN54LS689 . . . J PACKAGE
SN74LS688, SN74LS689 . . . DW, J OR N PACKAGE
(TOP VIEW)



SN54LS688, SN54LS689 . . . FK PACKAGE
SN74LS688, SN74LS689 . . . FN PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

description

These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $\overline{P > Q}$ outputs and the 'LS682 thru 'LS687 provide $\overline{P = Q}$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS683, 'LS685, 'LS687, and 'LS689 have open-collector outputs. The 'LS682 and 'LS683 feature 20 kΩ pullup termination resistors on the Q inputs for analog or switch data.

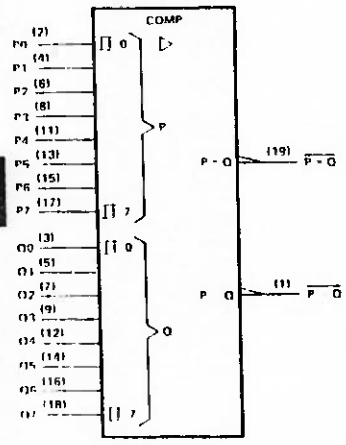
FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES			
P, Q	$\overline{G}$, $\overline{G1}$	$\overline{G2}$	$\overline{P = Q}$	$\overline{P > Q}$
P = Q	L	X	L	H
P > Q	X	L	H	L
P < Q	X	X	H	H
P = Q	H	X	H	H
P > Q	X	H	H	H
X	H	H	H	H

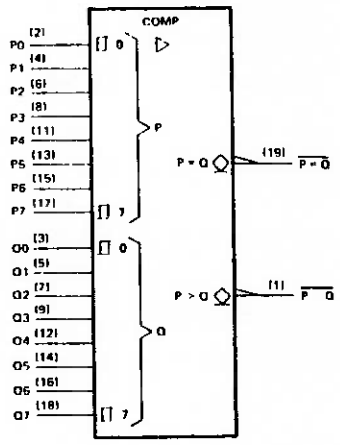
NOTES 1. The last three lines of the function table applies only to the devices having enable inputs, i.e., 'LS686 thru 'LS689.
2. The P < Q function can be generated by applying the P = Q and P > Q outputs to a 2-input NAND gate.
3. For 'LS686, 'LS687 G1 enables P > Q, and G2 enables P < Q.

logic symbols

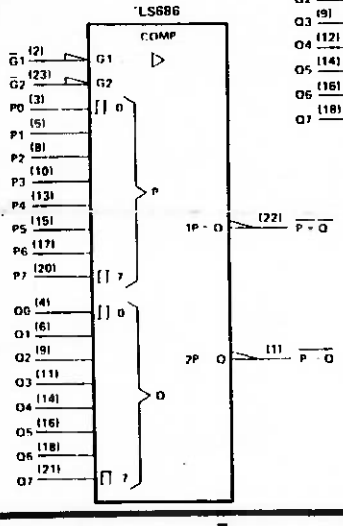
'LS682, 'LS684



'LS683, 'LS685

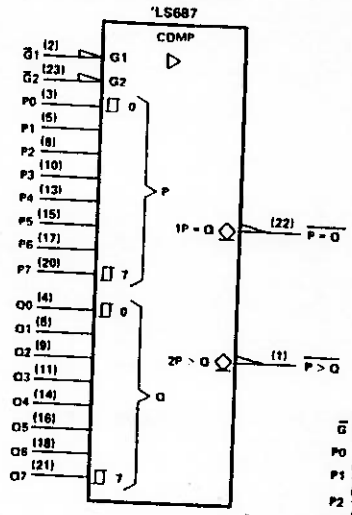


'LS686

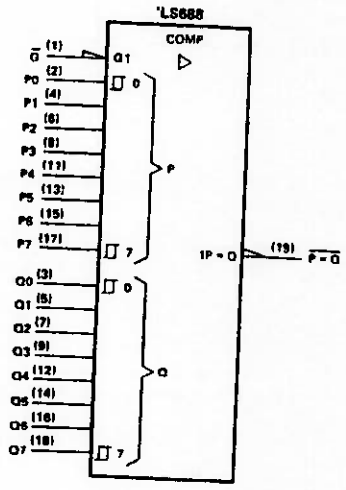


logic symbols (continued)

'LS687

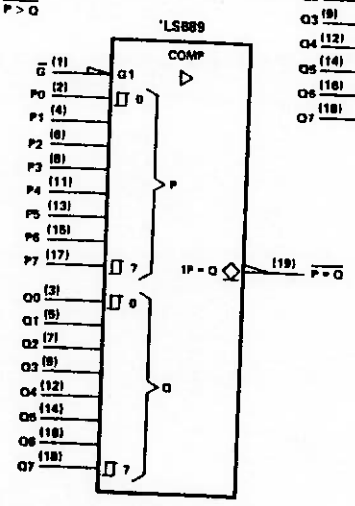


'LS688



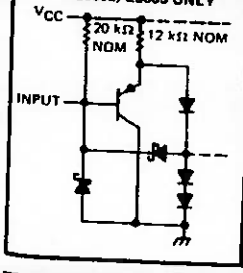
Pin numbers shown on logic notation are for DW, J, JT, N or NT packages

'LS689

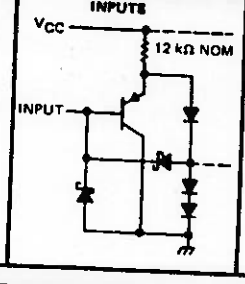


schematics of inputs and outputs

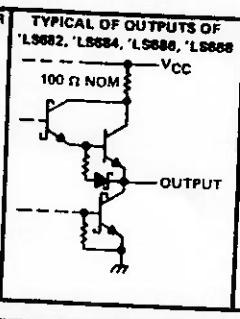
EQUIVALENT OF EACH Q INPUT OF 'LS682, LS683 ONLY



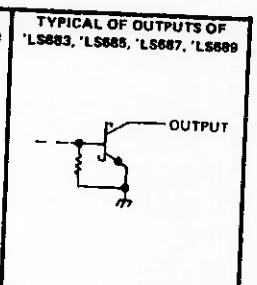
EQUIVALENT OF ALL OTHER INPUTS



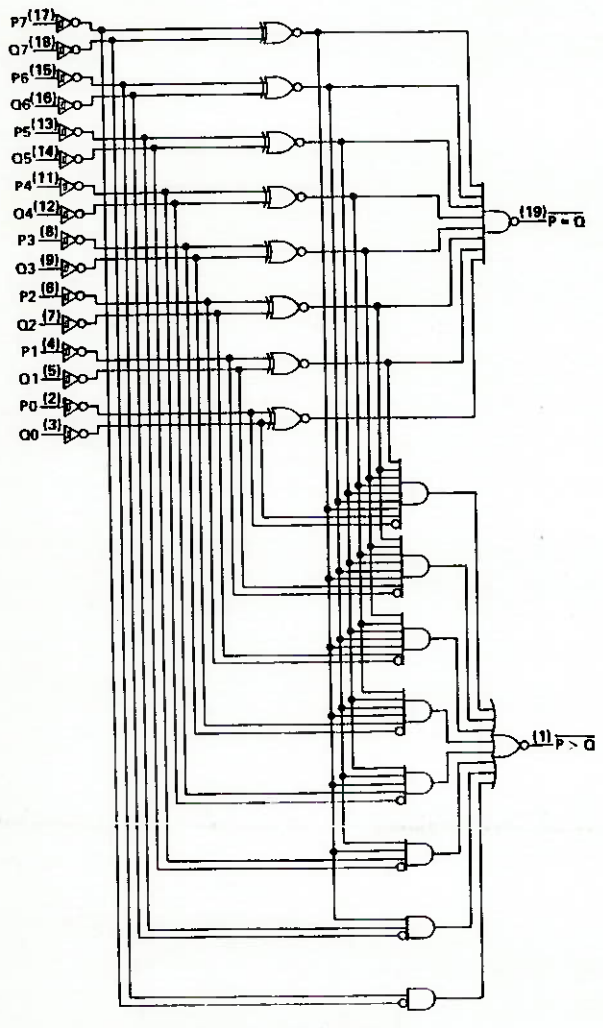
TYPICAL OF OUTPUTS OF 'LS682, 'LS684, 'LS686, 'LS688



TYPICAL OF OUTPUTS OF 'LS683, 'LS685, 'LS687, 'LS689



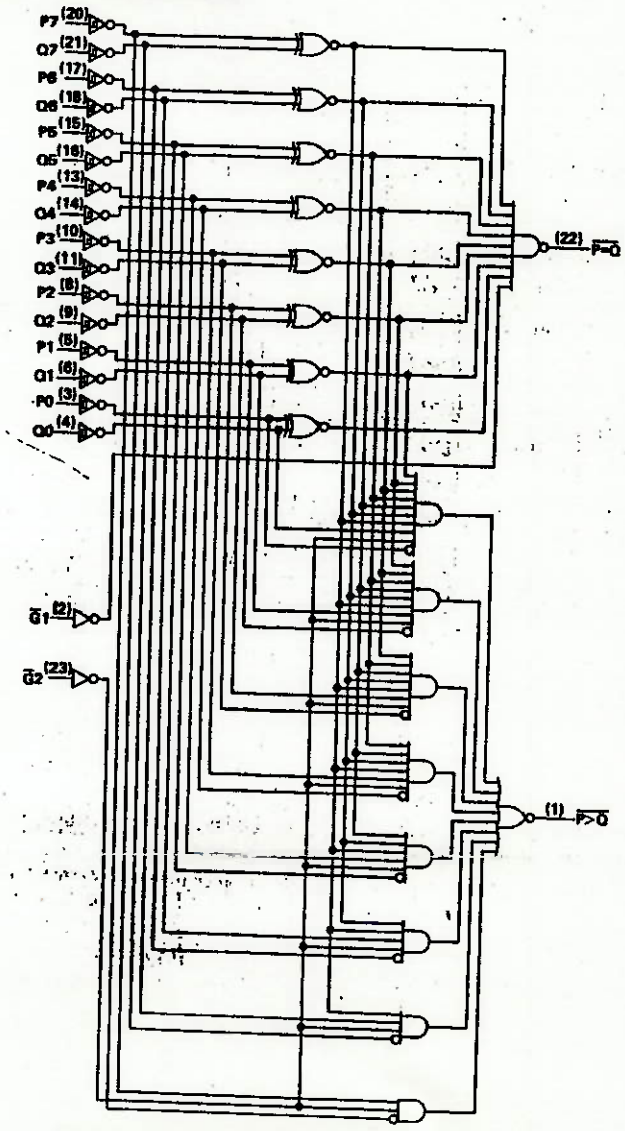
'LS682 thru 'LS685 logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, J or N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

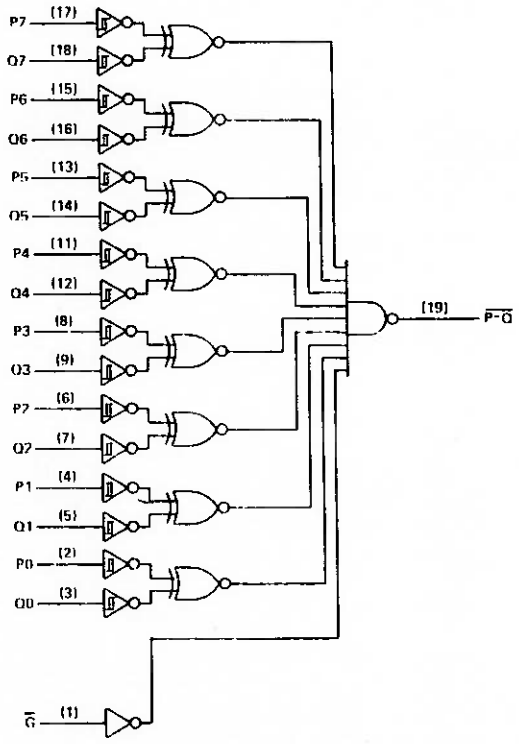
'LS686, 'LS687 logic diagram (positive logic)



Pin numbers shown on logic notation are for DW, JT, or NT packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'LS688, 'LS689 logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

absolute maximum ratings over operating free air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage: Q inputs of 'LS682 and 'LS683 . . . . . 5.5 V
All other inputs . . . . . 7 V
Off state output voltage: 'LS683, 'LS685, 'LS687, 'LS689 . . . . . 7 V
Operating free-air temperature range: SN54LS682 thru SN54LS689 . . . . . −55°C to 125°C
SN74LS682 thru SN74LS689 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

'LS682, 'LS684, 'LS686, 'LS688

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5			2.7			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	Q inputs, 'LS682	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{OS}§	Short-circuit output current		V_{CC} = MAX,	V_O = 0	−20		−100	−20		−100	mA
I_{CC}	Supply current	'LS682	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS684				40	65		40	65	
		'LS686				44	75		44	75	
		'LS688				40	65		40	65	

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with any G̅ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER#	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	P = Q	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		13	25		15	25		13	25		18	27	ns
t_{PHL}					15	25		17	25		20	30		20	30	
t_{PLH}	Q	P = Q			14	25		16	25		13	25		18	27	ns
t_{PHL}					15	25		15	25		21	30		20	30	
t_{PLH}	G̅, G̅1	P = Q									11	20		12	18	ns
t_{PHL}											19	30		13	20	
t_{PLH}	P	P > Q			20	30		22	30		19	30				ns
t_{PHL}					16	30		17	30		15	30				
t_{PLH}	Q	P > Q			21	30		24	30		18	30				ns
t_{PHL}					19	30		20	30		19	30				
t_{PLH}	G̅2	P > Q									21	30				ns
t_{PHL}											16	25				

#t_{PLH} = propagation delay time, low to high level output, t_{PHL} = propagation delay time, high to low level output.
NOTE 3: See General Information Section for load circuits and voltage waveforms.

recommended operating conditions 'LS683, 'LS685, 'LS687, 'LS689

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs	V_{CC} = MIN			0.4			0.4		V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL}max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			100	µA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		All other inputs	V_{CC} = MAX,	V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.7 V			20			20	µA
I_{IL}	Low-level input current	Q inputs, 'LS683	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		All other inputs					−0.2			−0.2	
I_{CC}	Supply current	'LS683	V_{CC} = MAX,	See Note 2		42	70		42	70	mA
		'LS685				40	65		40	65	
		'LS687				44	75		44	75	
		'LS689				40	65		40	65	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with any $\overline{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS683			'LS685			'LS687			'LS689			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$\overline{P}$ = $\overline{Q}$	R_L = 667 Ω, C_L = 45 pF, All other inputs low, See Note 3		30	45		30	45		24	35		24	40	ns
t_{PHL}					20	30		19	35		20	30		22	35	
t_{PLH}	Q	$\overline{P}$ = $\overline{Q}$			24	35		24	45		24	35		24	40	ns
t_{PHL}					23	35		23	35		20	30		22	35	
t_{PLH}	G, $\overline{G}$1	$\overline{P}$ = $\overline{Q}$									21	35		22	35	ns
t_{PHL}											18	30		19	30	
t_{PLH}	P	$\overline{P}$ < $\overline{Q}$			31	45		32	45		24	35				ns
t_{PHL}					17	30		16	35		18	30				
t_{PLH}	Q	$\overline{P}$ < $\overline{Q}$			30	45		30	45		24	35				ns
t_{PHL}					21	30		20	35		18	30				
t_{PLH}	$\overline{G}$2	$\overline{P}$ < $\overline{Q}$									24	35				ns
t_{PHL}											15	30				

*t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 3: See General Information Section for load circuits and voltage waveforms.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

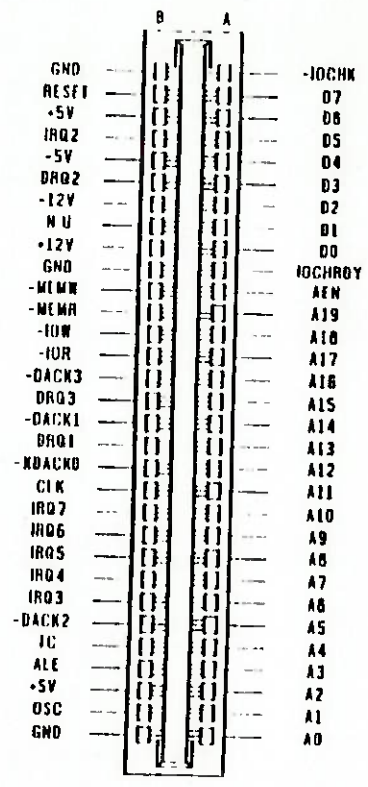
CONECTORES

Os conectores da placa CPU-III e suas respectivas relações de sinais são mostrados a seguir.

1 Conectores de Expansão

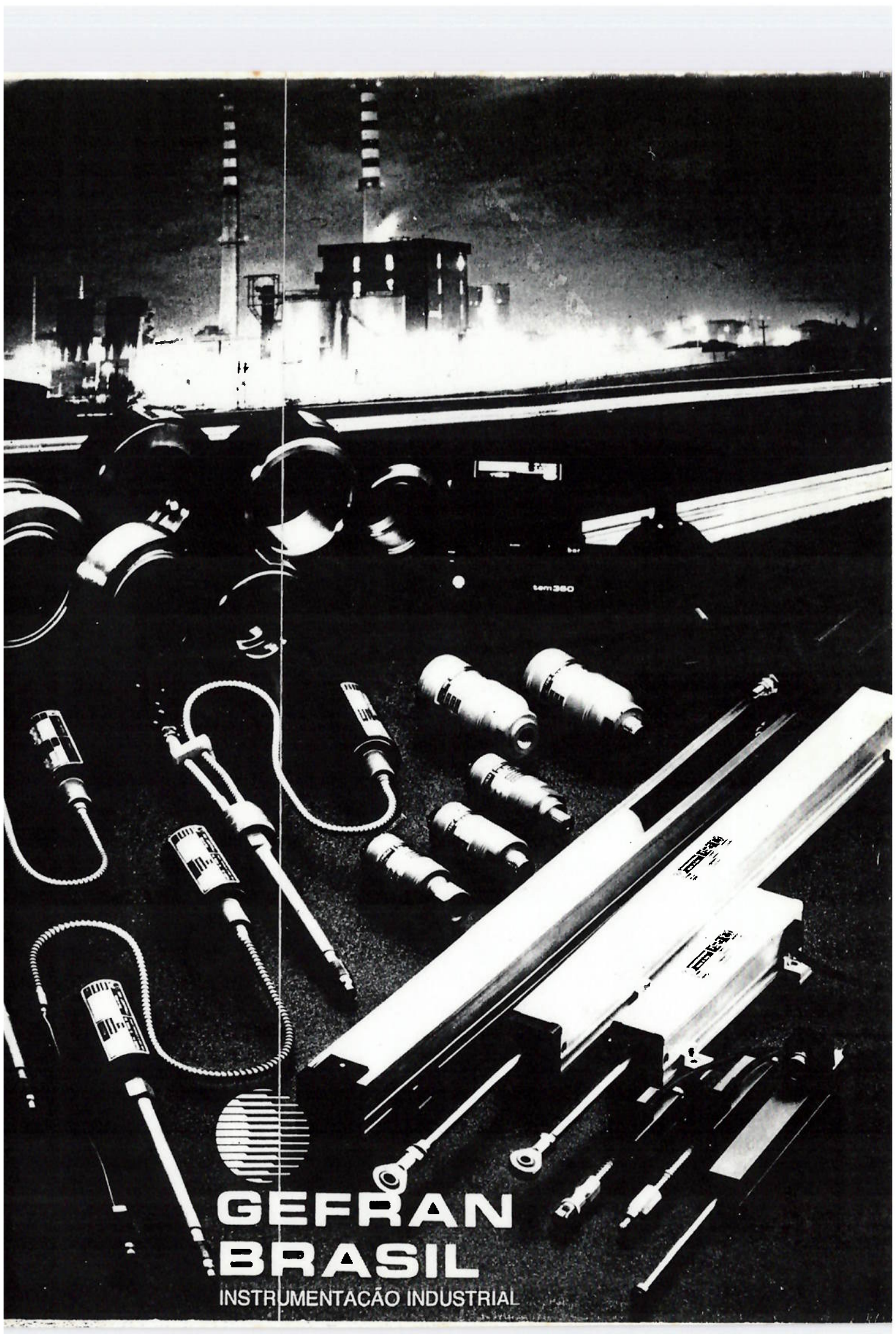
A placa CPU-III possue 8 conectores de expansão totalmente compatíveis com os dos microcomputadores IBM-PC e IBM-PC-XT.

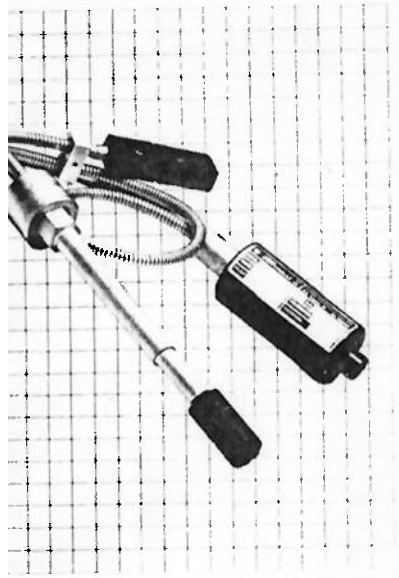
Estes conectores são identificados como CN10-F, CN11-F, CN12-F, CN13-F, CN15-F, CN16-F, CN18-F e CN19-F, mostrados a seguir:



Anexo 4

Catálogos


GEFRAN
BRASIL
INSTRUMENTACÃO INDUSTRIAL



TRANSDUTOR DE PRESSÃO ALTA TEMPERATURA SÉRIE SP

Os Transdutores de Pressão para Alta Temperatura série SP foram projetados para utilização na indústria de polímeros. Podem ser fornecidos em três classes de precisão, com diafragma em aço inox 17-4 PH ou Hastelloy C-4 e com sinal de saída em mV ou amplificado.

Campo de Medição	0-35 a 0-2000 bar		
Erro Combinado	< 0,5% – 1% – 2% F.E.		
Máxima Temperatura do Fluido	400°C		
Sensibilidade	2,5 – 3,3 mV/V		
	0-1/0-5/0-10 Vdc	0-20/4-20 mA	
Tensão de Alimentação	7 a 10 Vdc	15 a 30 Vdc	
Rosca	1/2-20 UNF	M14x1,5	M18x1,5
Princípio de Medição	Strain Gage		

TRANSDUTOR DE PRESSÃO A FILME FINO SÉRIE TF

Os Transdutores de Pressão Série TF são produzidos com tecnologia de Filme Fino, onde o extensômetro é depositado a alto vácuo diretamente sobre a membrana sensora, o que lhes confere uma vida elevada, ausência de creep e alta estabilidade.

Campo de Medição	0-50 a 0-700 bar
Erro Combinado	< 0,5% F.E.
Erro de Repetibilidade	< 0,1% F.E.
Sensibilidade	3 mV/V
Temperatura de Utilização	-20 a +120°C
Material do Elemento Sensor	Aço Inox 17-4 PH

TRANSDUTOR DE PRESSÃO SÉRIE TP

Os Transdutores de Pressão Série TP possuem princípio de medição por Strain Gage. Podem ser fornecidos com membrana interna e sinal de saída em mV (TP-86) ou amplificado (TP-89), ou com membrana rasante e sinal de saída em mV (TPF-86) ou amplificado (TPF-89).

Campo de Medição	0-10 a 0-2000 bar	
Erro Combinado	< 0,25% – 0,5% – 1% F.E.	
Erro de Repetibilidade	< 0,1% F.E.	
Sensibilidade TP-86 e TPF-86	3 mV/V	
TP-89 e TPF-89	0-1/0-5/0-10 Vdc	0-20/4-20 mA
Temperatura de Utilização	-30 a +100°C	
Material do Elemento Sensor	Aço Inox 17-4 PH	

CÉLULAS DE CARGA MODELOS CM, TC E TH

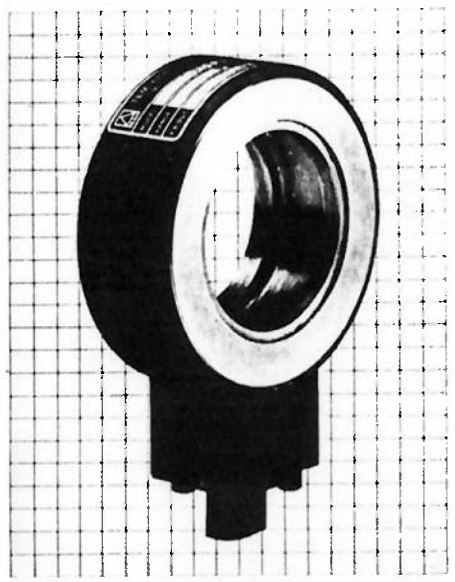
As Células de Carga Modelo CM, TC e TH possuem princípio de medição por Strain Gage e podem ser utilizadas para pesagem industrial, automação, laboratórios de testes, etc.

Campo de Medição	0-100 a 0-5000 kgf
Erro Combinado	< 0,2% – 0,1% F.E.
Erro de Repetibilidade	< 0,01% F.E.
Sensibilidade	2 – 3 mV/V
Temperatura de Utilização	-20 a +100°C
Material	Aço Inox 17-4 PH

CÉLULAS DE CARGA MODELO SH

As Células de Carga Modelo SH são ideais para utilização em pesagens industriais. Possuem corpo robusto e compacto e princípio de medição por Strain Gage.

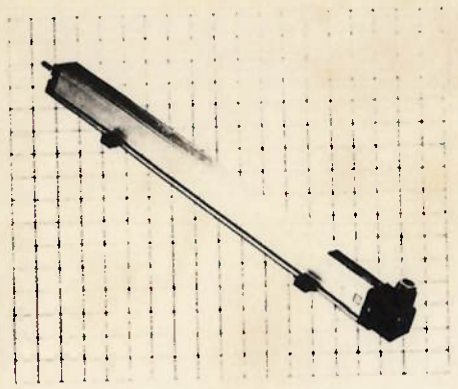
Campo de medição	0-5 a 0-30 kN
Erro Combinado	< 0,05% F.E.
Erro de Repetibilidade	< 0,01% F.E.
Sensibilidade	2 mV/V
Temperatura de Utilização	-20 a + 80 °C
Material	Aço Inox 17-4 PH



CÉLULAS DE CARGA TOROIDAIS MODELOS CT E CTS

As Células de Carga Toroidais possuem princípio de medição por Strain Gage e podem ser instaladas em colunas de máquinas. As células modelo CT podem ser utilizadas em extrusoras para monitorar indiretamente a pressão através da força de reação e as modelo CTS em máquinas injetoras para monitorar a tensão das colunas, entre outras aplicações.

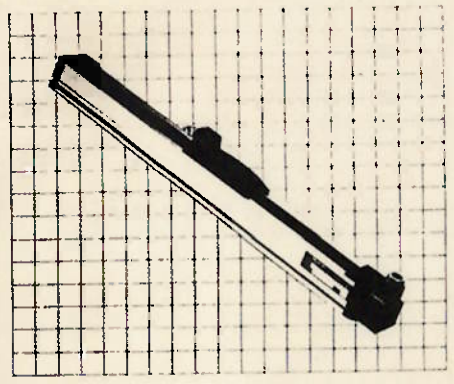
Campo de Medição	0-10 a 0-300 tf
Erro Combinado	< 0,5% F.E.
Erro de Repetibilidade	< 0,15% F.E.
Sensibilidade	2 mV/V
Temperatura de Utilização	-20 a + 100°C
Material	Aço Inox 17-4 PH



TRANSDUTORES LINEARES DE POSIÇÃO MODELO LT

Os Transdutores Modelo LT são potenciômetros lineares com pista plástica condutiva, indicados para medição e controle de posição e deslocamentos até 900 mm.

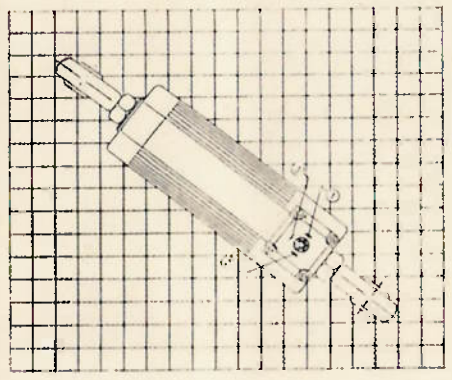
Curso Elétrico	0-50 a 0-900 mm
Resistência	5 ou 10 kΩ (dependendo do curso)
Erro de Linearidade	< ± 0,05% F.E.
Vida	> $100x10^6$ deslocamentos
Velocidade de Acionamento	⩽ 5m/s (10m/s opcional)



TRANSDUTORES LINEARES DE POSIÇÃO MODELO PK

Os Transdutores Modelo PK são potenciômetros lineares com pista plástica condutiva com saída lateral do cursor, indicados para medição e controle de posição e deslocamentos até 2000mm.

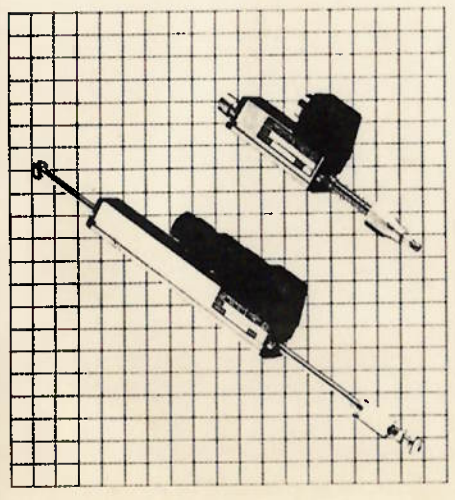
Curso Elétrico	0-100 a 0-2000 mm
Resistência	5 ou 10 ou 20 kΩ (dependendo do curso)
Erro de Linearidade	< ± 0,1% – ± 0,05% F.E.
Vida	> $100x10^6$ deslocamentos ou > $25x10^6$m
Velocidade de Acionamento	< 10 m/s



TRANSDUTORES LINEARES DE POSIÇÃO MODELO PC

Os Transdutores Modelo PC são potenciômetros lineares com pista plástica condutiva, com articulação nas duas extremidades para fixação, indicados para medição e controle de posição e deslocamentos até 750mm.

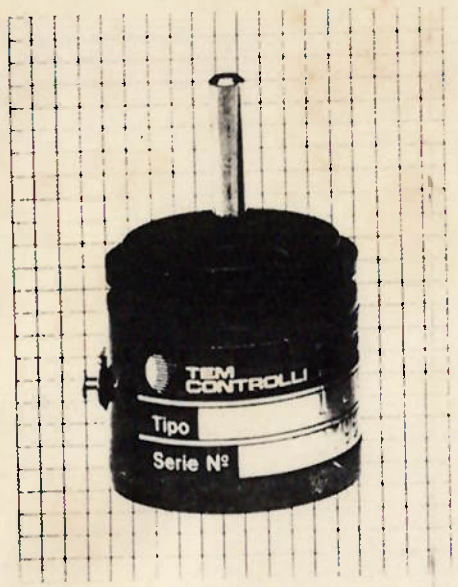
Curso Elétrico	0-50 a 0-750 mm
Resistência	5 ou 10 kΩ (dependendo do curso)
Erro de Linearidade	< ± 0,05% F.E.
Vida	> $100x10^6$ deslocamentos
Velocidade de Acionamento	< 5 m/s



TRANSDUTORES LINEARES DE POSIÇÃO PY1, PY2 E PY3

Os Transdutores Modelo PY são potenciômetros lineares com pista plástica condutiva, indicados para medição e controle de posição e pequenos deslocamentos mecânicos. O modelo PY1 possui um acoplamento esférico que elimina esforços em montagens desalinhadas. Os modelos PY2 e PY3 são apalpadores lineares, sendo que o primeiro possui uma esfera e o segundo um rolete na extremidade da haste.

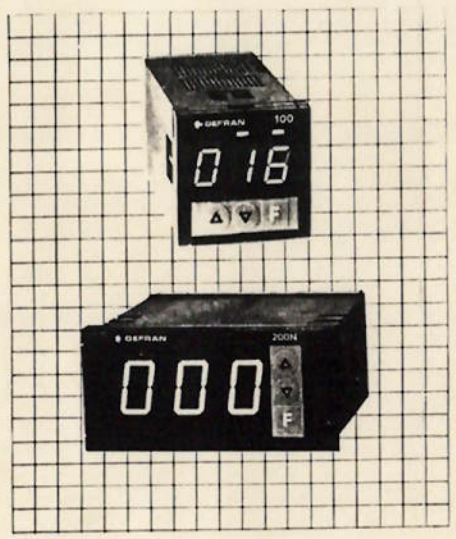
Curso Elétrico	0-25 a 0-150 mm
Resistência	1 ou 5 kΩ (dependendo do curso)
Erro de Linearidade	< ± 0,1% – ± 0,2% F.E.
Vida	$100x10^6$ deslocamentos
Velocidade de Acionamento	< 10 m/s



TRANSDUTORES ROTATIVOS DE POSIÇÃO SÉRIE PS

Os Transdutores Série PS são potenciômetros rotativos com pista plástica condutiva, indicados para medição e controle de posição e deslocamentos angulares.

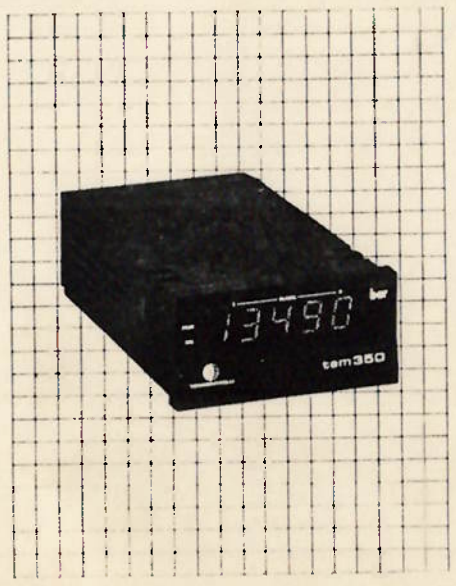
Curso Elétrico	340° – 345° – 350°
Resistência	1 ou 4,7 ou 10 kΩ
Erro de Linearidade	< 0,5% F.E.
Vida	> $20x10^6$ operações
Máxima Rotação	600 RPM



INDICADOR DIGITAL MICROPROCESSADO MODELO 100/200/201

Os Instrumentos modelo 100, 200 e 201 são indicadores digitais microprocessados para painel de 3 dígitos (100 e 200) e 3 1/2 dígitos (201), com até 4 alarmes através de relés, totalmente configuráveis, com possibilidade de saída de 24 Vdc para alimentação de transmissores. Possuem entrada para sinais de termopar, termo-resistência, potenciômetros e sinais em corrente e tensão dc.

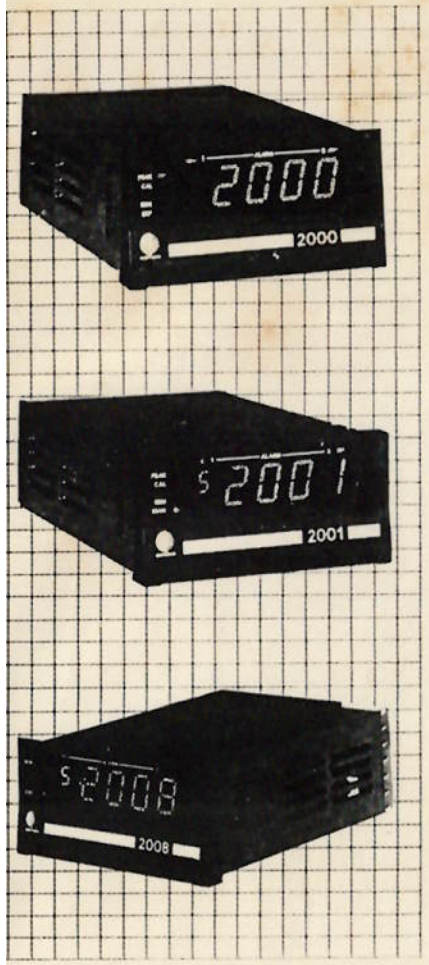
Entrada	Termopar tipo J/K/S/T Tensão 0-50mV, 0-10Vdc Potenciômetro 2 a 20 kΩ	Termo-resistência Pt100 Corrente 0-20/4-20mA
Alarme	até 4 alarmes através de relés	
Alimentação para Transmissor	24Vdc/30mA (modelos 200 e 201)	
Display	3 dígitos (100 e 200)	3 1/2 dígitos (201)
Alimentação	100/220Vac	24/240Vac 50/60Hz
Dimensão	100: 48x48mm	200 e 201: 96x48mm



INDICADOR DIGITAL MODELO TEM 350

O Instrumento TEM 350 é um indicador para painel projetado para monitorar sinais de transdutores de pressão e células de carga a strain gage, transdutores de posição resistivos e sinais em tensão e corrente dc. Possui duas saídas de alarme através de relés com ajuste local ou remoto, duas saídas auxiliares, uma em tensão e outra em corrente, memória de pico máximo e ajuste de zero e ganho através de potenciômetro no painel frontal.

Entrada	Strain Gage R ⩾ 350 Ω Corrente 0-20/4-20 mA	Potenciômetro R ⩾ 500 Ω Tensão 5 mV a 10Vdc
Alimentação para Transdutor	10Vdc/40mA ou 15Vdc/40mA	
Display	3 1/2 dígitos	
Alarmes	2 alarmes através de relés ajustáveis na faixa de 0-100%	
Alimentação	110/220Vac ou 24/48Vac 50/60 Hz	
Dimensão	96x48x152mm (DIN 43700)	



INDICADOR DIGITAL SÉRIE 2000

O Instrumento Modelo 2000 é um indicador digital microprocessado para painel, com 3 1/2 dígitos, 2 saídas de alarme através de relés com ajuste local ou remoto, saída auxiliar em tensão ou corrente, memória de pico máximo, saída serial e rearme local ou remoto. Pode ser utilizado para monitorar sinais de sensores de temperatura, transdutores de pressão e células de carga a strain gage, transdutores de posição resistivos, sinais em corrente e tensão ac e dc e em frequência.
O Instrumento Modelo 2001 é um controlador digital microprocessado "single loop" de ação PI. Possui as mesmas características do modelo 2000, exceto para, medição de temperatura e sinais em tensão e corrente ac.
O Instrumento Modelo 2008, além de todas as características do modelo 2000, possui entrada para até 8 zonas de medição.
Através do módulo M8, pode-se expandir para até 10 o número de saídas de alarmes através de relés.

Entrada	Termopar tipo J/L/K/R/S/B/T	Termoresistência Pt100
	Strain Gage 1,5 a 3,3 mV/V	Potenciômetro R≥300Ω
	Tensão dc 20mV a 500V	Tensão ac 100mV a 500V
	Corrente dc 200 μA a 2A	Corrente ac 2mA a 5A
	Frequência 200Hz a 20kHz	

Alimentação para Transdutor	5 a 15 Vdc
Alarmes	2 alarmes através de relés ajustáveis na faixa de 0-100%
Display	3 1/2 dígitos
Alimentação	24/110/220Vac 50/60 Hz
Dimensão	96x48x152mm (DIN43700)

GEFRAN
BRASIL
INSTRUMENTAÇAO INDUSTRIAL

GEFRAN BRASIL ELETROELETRÔNICA LTDA.
Al. Barão de Limeira, 739 - S/1
01202 - São Paulo - SP
Tel.: 011 / 223-8827
Fax.: 011 / 223-8827

GRUPPO
GEFRAN
INDUSTRIAL ELETRONICS